Inv. № 540

4275K 5-V Low- Drop Voltage Regulator

December 2009

FEATURES

- Output voltage 5V ± 2%
- Very low current consumption
- Power-on and undervoltage reset
- Reset low down to V_Q = 1 V
- Very Low- drop voltage
- Short- circuit- proof
- Reverse polarity proof
- Suitable for use in automotive electronics

DESCRIPTION

The 4275K is a monolithic integrated low-drop voltage regulator in a 5 pin TO- package. An input voltage up to 45 V is regulated to V_Q = 5.0 V. The IC is able to drive loads up to 450 mA and is short- circuit proof. At over temperature the 4275K is disabled by the incorporated temperature protection. A reset signal is generated for an output voltage V_Q of typ.4.65 V. The delay time can be programmed by the external delay capacitor.

DIMENSIONING Information on External Components

The input capacitor C_I is necessary for compensating line influences. The output capacitor C_Q is necessary for the stability of the regulation circuit. Stability is guaranteed at values $C_Q \geq$ 22 µF and an ESR of ≤ 5 Ω within the operating temperature range.

Circuit Description

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The IC also incorporates a number of internal circuits for protection against:

- Overload
- Over- temperature
- Reverse polarity

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PIN CONFIGURATION

(top view)

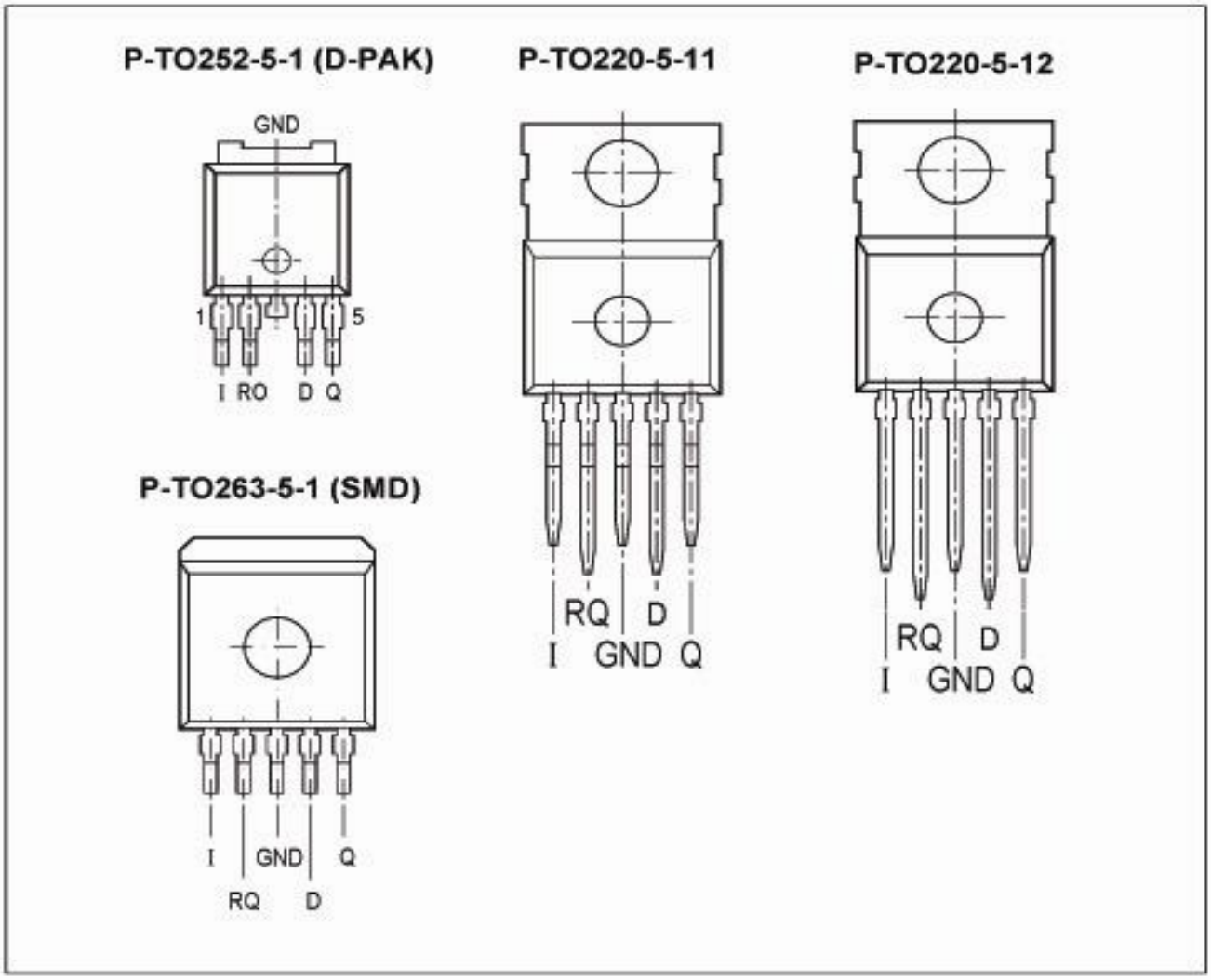

Figure 1.

Pin Definitions and Functions

Pin No	Symbol	Function
1	I	**Input**; block to ground directly at the IC with a ceramic capacitor
2	RQ	**Reset Output**; open collector output
3	GND	**Ground**; Pin 3 internally connected to heatsink
4	D	**Reset Delay**; connected capacitor to GND for setting delay time
5	Q	**Output**; block to ground with a ≥ 22 µF capacitor, ESR < 5 Ω at 10 kHz

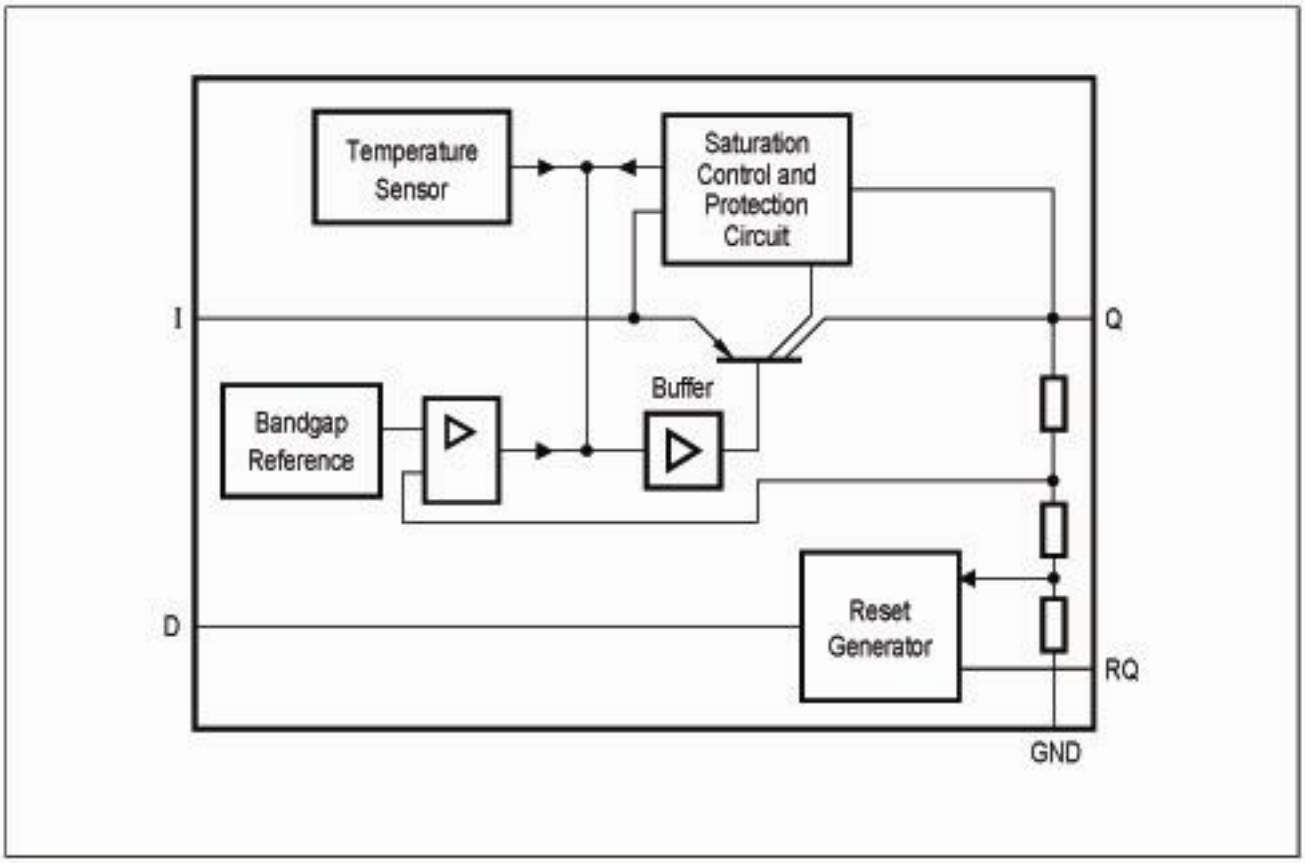

Figure 2.
Block Diagram

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ABSOLUTE MAXIMUM RATINGS

T_j = - 40 to 150 ºC

Parameter	Symbol	Limit Values		Unit	Test Condition
		min	max		
Voltage Regulator Input					
Voltage	V_I	- 42	45	V	-
Current	I_I	-	-	-	Internally limited
Output					
Voltage	V_Q	- 1.0	16	V	-
Current	I_Q	-			Internally limited
Reset Output					
Voltage	V_{RO}	- 0.3	25	V	-
Current	I_{RO}	- 5	5	mA	-
Reset Delay					
Voltage	v_D	- 0.3	7	V	-
Current	I_D	- 2	2	mA	-
Temperature					
Junction temperature	T_J	-	150	ºC	-
Storage temperature	T_{stg}	- 50	150	ºC	-

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

OPERATING RANGE

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Input voltage	V_I	5.5	42	V	-
Junction temperature	T_J	- 40	150	ºC	-

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CHARACTERISTICS

V_I = 13.5 V; - 40 °C <T_J <150 °C (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		min	typ	max		
Output						
Output voltage	V_Q	4.9	5.0	5.1	V	5ma < I_Q < 400 mA 6V < V_I < 40 V
Output current limitation[1)]	I_Q	450	700	-	mA	-
Current consumption; $I_q = I_I - I_Q$	I_q	-	150	200	µA	I_Q = 1 mA T_I =25 °C
Current consumption; $I_q = I_I - I_Q$	I_q	-	150	220	µA	I_Q = 1 mA T_I ≤ 85 °C
Current consumption; $I_q = I_I - I_Q$	I_q I_q	-	5 12	10 22	mA	I_Q = 250 mA I_Q = 400 mA
Drop voltage [1)]	V_{dr}	-	250	500	mV	I_Q = 300 mA $V_{dr} = V_I – V_Q$
Load regulation	ΔV_Q	-	15	30	mV	I_Q = 5 mA to 400 mA
Line regulation	ΔV_Q	-15	5	15	mV	ΔV_I = 8 V to 32 V I_Q = 5 mA

CHARACTERISTICS (cont' d)

V_I = 13.5 V; - 40 °C< T_J < 150 °C (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		min	typ	max		
Power supply ripple rejection	PSRR	-	60	-	dB	F_r = 100 Hz Vr = 0.5 Vpp
Temperature output Voltage drift	dV_Q/dT	-	0.5	-	mV/K	-
Reset Timing D and Output RQ						
Reset switching threshold	V_{RT}	4.5	4.65	4.8	V	-
Reset output low voltage	V_{RQL}	-	0.2	0.4	V	R_{ext} ≥ 5Ω, V_Q > 1 V
Reset output leakage current	I_{RQH}	-	0	2	µA	V_{RQH} > 4.5 V
Reset charging current	Id	3	6	9	µA	V_D = 1 V
Upper timing threshold	V_{DU}	1.5	1.8	2.2	V	-
Lower timing threshold	V_{DL}	0.2	0.4	0.7	V	-
Reset delay time	T_D	10	16	22	ms	C_D = 47nF
Reset reaction time	T_{RR}	-	0.5	2	µs	C_D = 47nF

1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I =13.5 V

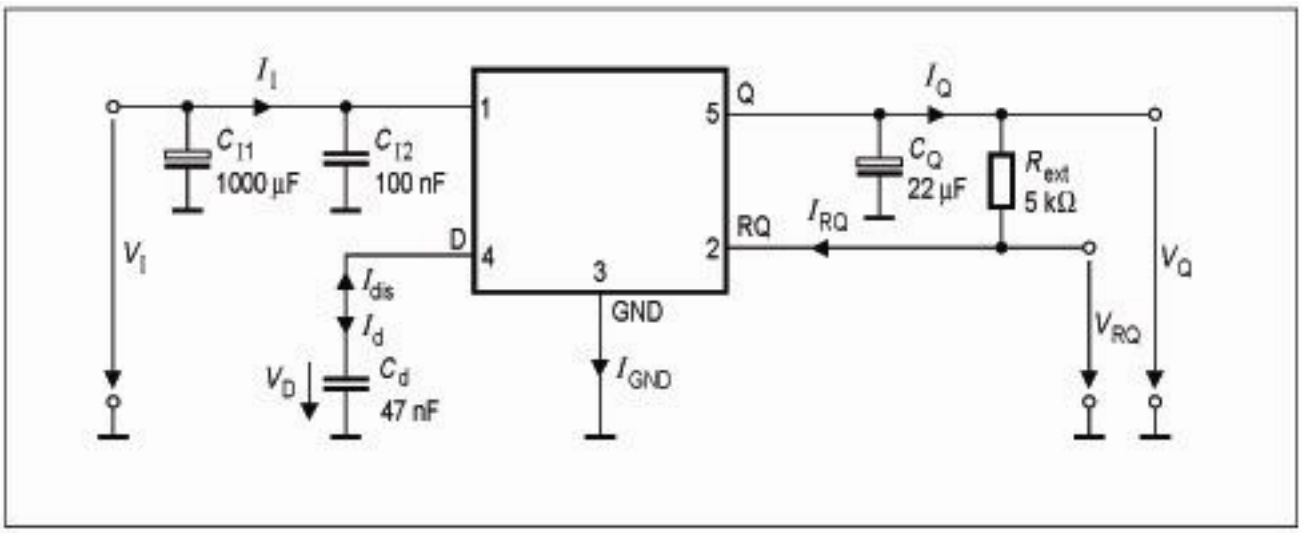


Figure 3. **Test Circuit**

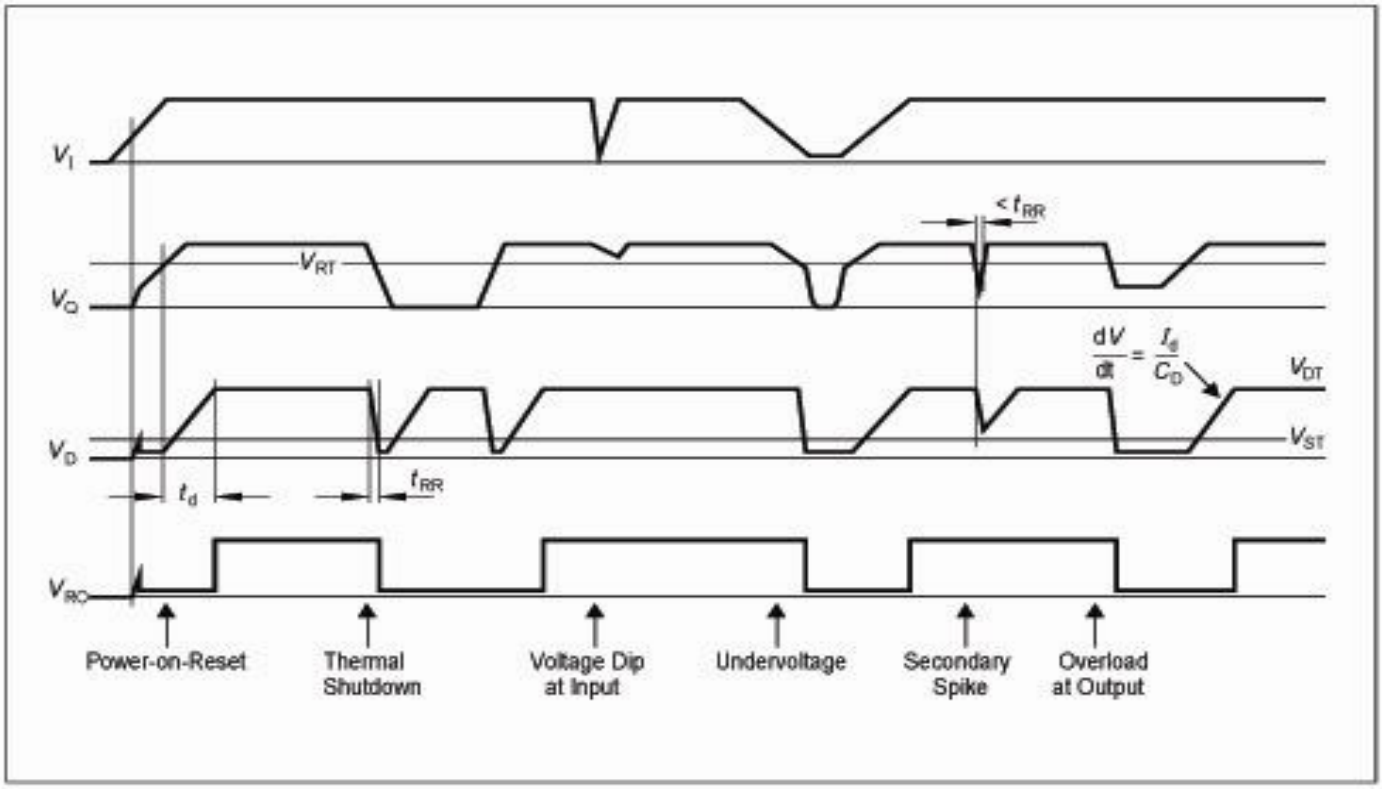
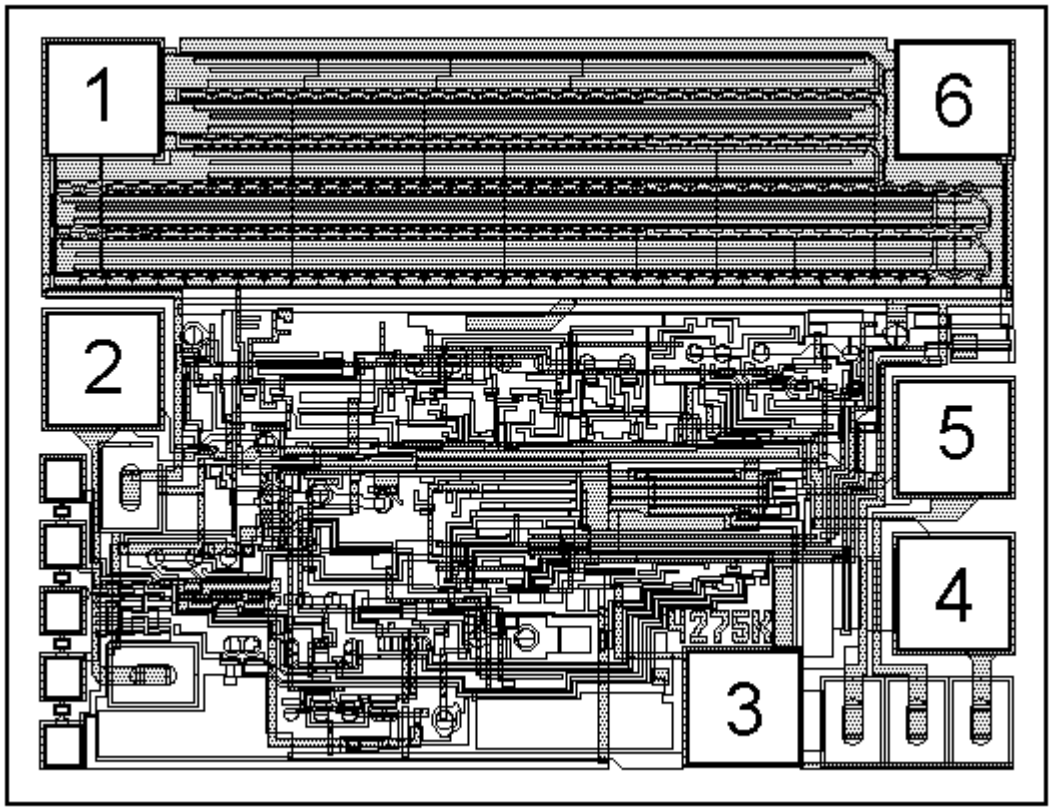


Figure 4 Reset Timing

PAD LOCATION 4275K

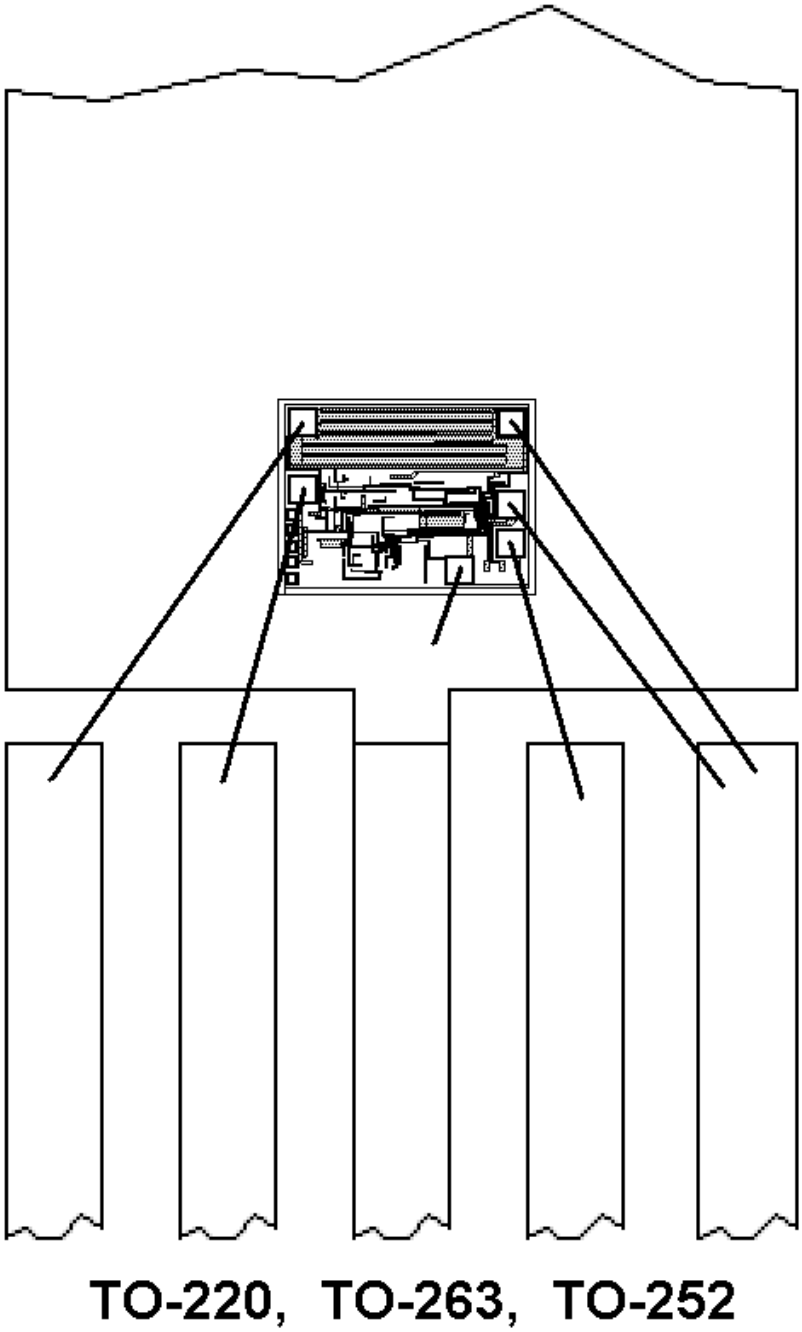


Chip size 1.73 x 1.33 mm^2

Pad Name and Coordinates

Pad No	Pad Name	Pad Opening Size (μm)	Pad Center Coordinates (μm)	
			X	Y
1	Input	190*190	160	1170
2	Reset Output	190*190	160	720
3	GND	190*190	1220	160
4	Reset Delay	190*190	1570	350
5	Output	190*190	1570	610
6	Output	190*190	1570	1170

4275K
Drawing Assembly



The appearance complies with the requirements of the company standards