# 4523K Wide-Input Sensorless CC/CV Step-Down DC/DC Converter

Preliminary May 2014

## GENERAL DESCRIPTION

4523K is a wide input voltage, high efficiency Active CC step-down DC/DC converter that operates in either CV (Constant Output Voltage) mode or CC (Constant Output Current) mode. 4523K provides up to 3A output current at 225kHz switching frequency.
Active CC eliminates the expensive,high accuracy current sense resistor, making it ideal for battery charging applications and adaptors with accurate current limit.
Protection features include cycle-by-cycle current limit, thermal shutdown, and frequency foldback at short circuit. The devices are available in a SOP- 8EP package and require very few external devices for operation.

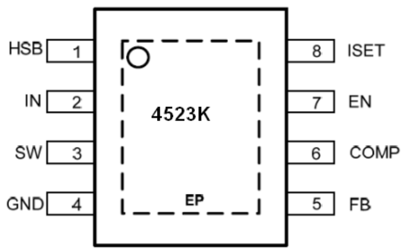
## FEATURES

- 40V Input Voltage Surge
- 38V Steady State Operation
- Up to 3A output current
- Output Voltage up to 12V
- CC Sensorless Constant Current Control
- Resistor Programmable
  - − Current Limit from 1.5A to 3A
  - − Cable Compensation from 0Ω to 0.3Ω
- ±7.5% CC Accuracy
- 2% Feedback Voltage Accuracy
- Up to 94% Efficiency
- 225kHz Switching Frequency Eases EMI Design
- Advanced Feature Set
  - − Integrated Soft Start
  - − Thermal Shutdown
  - − Secondary Cycle-by-Cycle Current Limit
  - − Protection Against Shorted ISET Pin
- SOP-8EP Package

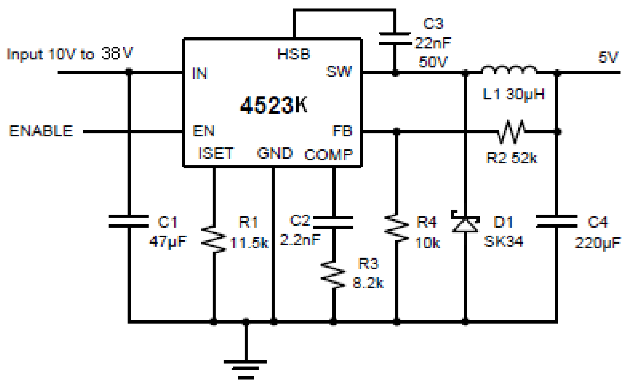
## APPLICATIONS

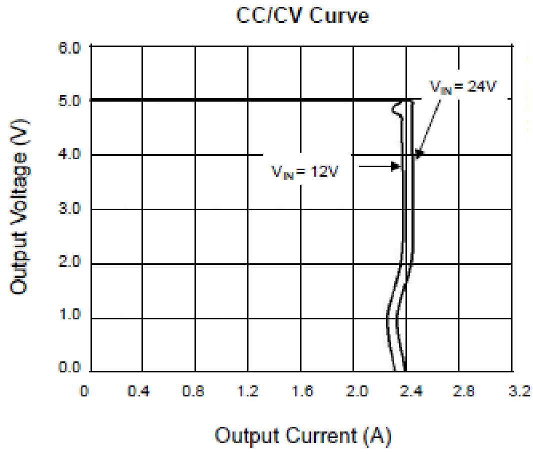
- Car Charger/ Adaptor
- Rechargeable Portable Devices
- General- Purpose CC/CV Supply

PIN CONFIGURATION




SOP-8EP




## PIN DESCRIPTIONS

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | HSB | High Side Bias Pin. This provides power to the internal high-side MOSFET gate driver. Connect a 22nF capacitor from HSB pin to SW pin. |
| 2 | IN | Power Supply Input. Bypass this pin with a 10µF ceramic capacitor to GND, placed as close to the IC as possible. |
| 3 | SW | Power Switching Output to External Inductor. |
| 4 | GND | Ground. Connect this pin to a large PCB copper area for best heat dissipation. Return FB, COMP, and ISET to this GND, and connect this GND to power GND at a single point for best noise immunity. |
| 5 | FB | Feedback Input. The voltage at this pin is regulated to 0.808V. Connect to the resistor divider between output and GND to set the output voltage. |
| 6 | COMP | Error Amplifier Output. This pin is used to compensate the converter. |
| 7 | EN | Enable Input. EN is pulled up to 5V with a 4µA current, and contains a precise 1.6V logic threshold. Drive this pin to a logic-high or leave unconnected to enable the IC. Drive to a logic-low to disable the IC and enter shutdown mode. |
| 8 | ISET | Output Current Setting Pin. Connect a resistor from ISET to GND to program the output current. |
| | Exposed Pad | Heat Dissipation Pad. Connect this exposed pad to large ground copper area with copper and vias. |

## ABSOLUTE MAXIMUM RATINGS

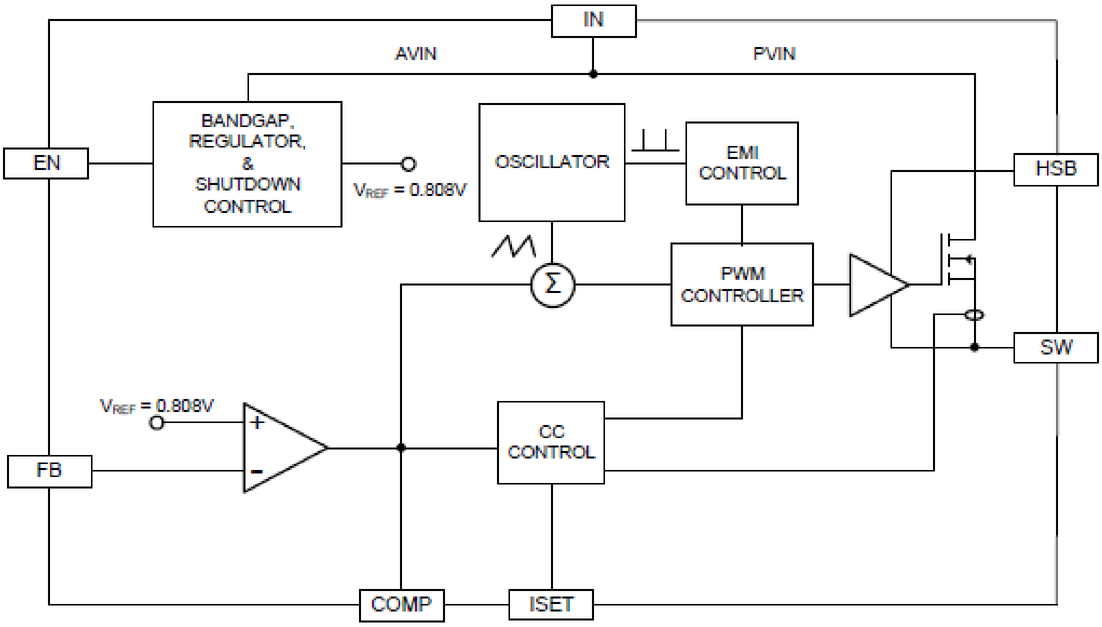
| PARAMETER | VALUE | UNIT |
|---|---|---|
| IN to GND | -0.3 to 40 | V |
| SW to GND | -1 to $V_{IN}$ + 1 | V |
| HSB to GND | $V_{SW}$ - 0.3 to $V_{SW}$ + 7 | V |
| FB, EN, ISET, COMP to GND | -0.3 to + 6 | V |
| Junction to Ambient Thermal Resistance | 46 | °C/W |
| Operating Junction Temperature | -40 to 150 | °C |

## ELECTRICAL CHARACTERISTICS

($V_{IN}$ = 20V, $T_A$ = 25°C, unless otherwise specified)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input Voltage | | 10 | | 38 | V |
| Input Voltage Surge | | | | 40 | V |
| $V_{IN}$ UVLO Turn-On Voltage | Input Voltage Rising | 9.0 | 9.4 | 9.7 | V |
| $V_{IN}$ UVLO Hysteresis | Input Voltage Falling | | 1.1 | | V |
| Standby Supply Current | $V_{EN}$ = 3V, $V_{FB}$ = 1V | | 0.9 | 1.4 | mA |
| | $V_{EN}$ = 3V, $V_{OUT}$ = 5V, No load | | 3.0 | | mA |
| Shutdown Supply Current | $V_{EN}$ = 0V | | 75 | 115 | µA |
| Feedback Voltage | | 792 | 808 | 824 | mV |
| Internal Soft-Start Time | | | 550 | | µs |
| Error Amplifier Transconductance | $V_{COMP}$ = 1.6V, $\Delta I_{COMP}$ = ± 10µA | | 700 | | µA/V |
| Error Amplifier DC Gain | | | 4000 | | V/V |
| Switching Frequency | $V_{FB}$ = 0.808V | 200 | 225 | 250 | kHz |
| Foldback Switching Frequency | $V_{FB}$ = 0V | | 30 | | kHz |
| Maximum Duty Cycle | | 85 | 88 | 91 | % |
| Minimum On-Time | | | 200 | | ns |
| COMP to Current Limit Transconductance | $V_{COMP}$ = 1.2V | | 3.5 | | A/V |
| Secondary Cycle-by-Cycle Current Limit | Duty Cycle = 0% | | 4.5 | | A |
| Slope Compensation | Duty = $D_{MAX}$ | | 1.2 | | A |
| ISET Voltage | | | 1 | | V |
| ISET to IOUT DC Room Temp Current Gain | $I_{OUT}$ / $I_{SET}$, $R_{ISET}$ = 19.6kΩ | | 25000 | | A/A |
| CC Controller DC Accuracy | $R_{ISET}$ = 19.6kΩ, $V_{OUT}$ = 3.5V<br>Open-Loop DC Test | 1175 | 1190 | 1205 | mA |
| EN Threshold Voltage | EN Pin Rising | 1.47 | 1.6 | 1.73 | V |
| EN Hysteresis | EN Pin Falling | | 125 | | mV |
| EN Internal Pull-up Current | | | 4 | | µA |
| High-Side Switch ON-Resistance | | | 0.16 | | Ohm |
| SW Off Leakage Current | $V_{EN}$ = $V_{SW}$ = 0V | | 1 | 10 | µA |
| Thermal Shutdown Temperature | Temperature Rising | | 150 | | °C |
| Thermal Shutdown Temperature Hysteresis | Temperature Falling | | 20 | | °C |

## FUNCTIONAL BLOCK DIAGRAM




## FUNCTIONAL DESCRIPTION

### CV/CC Loop Regulation

As seen in Functional Block Diagram, the 4523K is a peak current mode pulse width modulation (PWM) converter with CC and CV control. The converter operates as follows:

A switching cycle starts when the rising edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy in the magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes low, the High-Side Power Switch turns off.

At this point, the SW side of the inductor swings to a diode voltage below ground, causing the inductor current to decrease and magnetic energy to be transferred to output. This state continues until the cycle starts again. The High-Side Power Switch is driven by logic using HSB as the positive rail. This pin is charged to $V_{SW}$ + 5V when the Low-Side Power Switch turns on.

The COMP voltage is the integration of the error between FB input and the internal 0.808V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output. Output current will increase until it reaches the CC limit set by the ISET resistor. At this point, the device will transition from regulating output voltage to regulating output current, and the output voltage will drop with increasing load.

The Oscillator normally switches at 225 kHz. However, if FB voltage is less than 0.6V, then the switching frequency decreases until it reaches a typical value of 30 kHz at $V_{FB}$ = 0.15V.

### Enable Pin

The 4523K has an enable input EN for turning the IC on or off. The EN pin contains a precision 1.6V comparator with 125mV hysteresis and a 4μA pull-up current source. The comparator can be used with a resistor divider from $V_{IN}$ to program a startup voltage higher than the normal UVLO value. It can be used with a resistor divider from $V_{OUT}$ to disable charging of a deeply discharged battery, or it can be used with a resistor divider containing a thermistor to provide a temperature-dependent shutoff protection for over temperature battery. The thermistor should be thermally coupled to the battery pack for this usage.

If left floating, the EN pin will be pulled up to roughly 5V by the internal 4μA current source. It can be driven from standard logic signals greater than 1.6V, or driven with open-drain logic to provide digital ON/OFF control.

### Thermal Shutdown

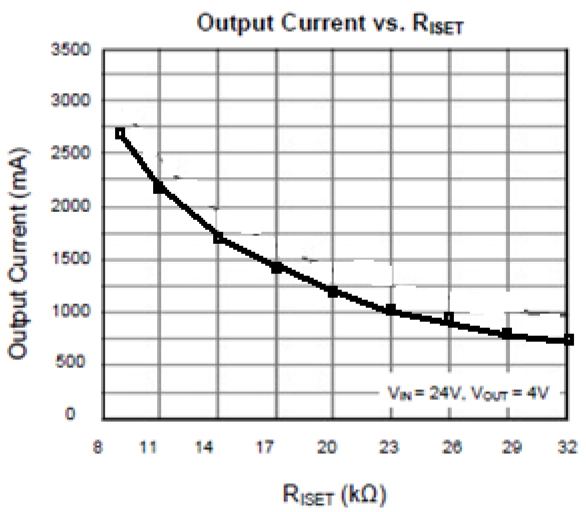
The 4523K disables switching when its junction temperature exceeds 150°C and resumes when the temperature has dropped by 20°C.

### CC Current Setting

4523K constant current value is set by a resistor connected between the ISET pin and GND. The CC output current is linearly proportional to the current flowing out of the ISET pin. The voltage at ISET is roughly 1V and the current gain from ISET to output is roughly 25000 (25mA/1µA). To determine the proper resistor for a desired current, please refer to Figure 1 below.

**Figure 1**

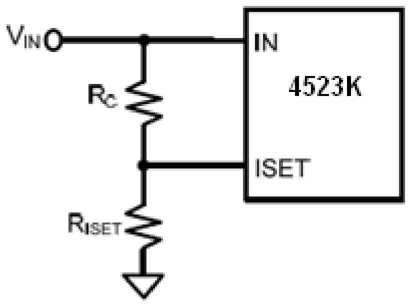
**Curve for Programming Output CC Current**




### CC Current Line Compensation

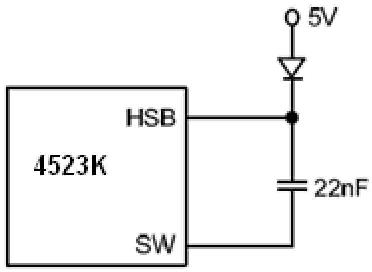
When operating at constant current mode, the current limit increase slightly with input voltage. For wide input voltage applications, a resistor $R_C$ is added to compensate line change and keep output high CC accuracy, as shown in Figure 2.

**Figure 2**
**Iutput Line Compensation**



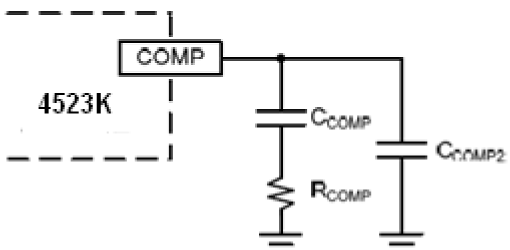

**External High Voltage Bias Diode**
It is recommended that an external High Voltage Bias diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The High Voltage Bias diode can be a low cost one such as IN4148 or BAT54.
This diode is also recommended for high duty cycle operation and high output voltage applications.

**Figure 3**
**External High Voltage Bias Diode**




## STABILITY COMPENSATION

**Figure 4**
**Stability Compensation**




$C_{COMP2}$ is needed only for high ESR output capacitor

The following steps should be used to compensate the IC:

**STEP 1**. Set the cross over frequency at 1/10 of the switching frequency via $R_{COMP}$:

$$R_{COMP} = \frac{2\pi V_{OUT} C_{OUT} f_{SW}}{10 G_{EA} G_{COMP} \times 0.808V}$$

$= 5.12 \times 10^7\ V_{OUT}\ C_{OUT}$ (Ω)

**STEP 2.** Set the zero $f_{Z1}$ at 1/4 of the cross over frequency. If $R_{COMP}$ is less than 15kΩ, the equation for $C_{COMP}$ is:

$$C_{COMP} = \frac{2.83 \times 10^5}{R_{COMP}} \quad \text{(F)}$$

If $R_{COMP}$ is limited to 15 kΩ, then actual cross over frequency is 6.58 / ($V_{OUT}C_{OUT}$).

Therefore: $C_{COMP} = 6.45 \times 10^{-6} V_{OUT}C_{OUT}$ (F)

**STEP 3**. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the cross over frequency, an additional compensation capacitor $C_{COMP2}$ is required. The condition for using $C_{COMP2}$ is:

$$R_{ESRCOUT} \geq (\mathrm{Min}\ \frac{1.77 \times 10^{-6}}{C_{OUT}},\ 0.006 \times V_{OUT})\ (\Omega)$$

And the proper value for $C_{COMP2}$ is:

$$C_{COMP2} = \frac{C_{OUT}R_{ESRCOUT}}{R_{COMP}}$$

Though $C_{COMP2}$ is unnecessary when the output capacitor has sufficiently low ESR, a small value $C_{COMP2}$ such as 100pF may improve stability against PCB layout parasitic effects.

Table 1 shows some calculated results based on the compensation method above.

### Table 1.
### Typical Compensation for Different Output Voltages and Output Capacitors

| $V_{OUT}$ | $C_{OUT}$ | $R_{COMP}$ | $C_{COMP}$ | $C_{COMP2}$* |
|---|---|---|---|---|
| 2.5V | 47µF Ceramic CAP | 5.6kΩ | 3.3nF | None |
| 3.3V | 47µF Ceramic CAP | 6.2kΩ | 3.3nF | None |
| 5V | 47µF Ceramic CAP | 8.2kΩ | 3.3nF | None |
| 2.5V | 47µF/6.3V/30mΩ | 39kΩ | 22nF | 47pF |
| 3.3V | 47µF/6.3V/30mΩ | 45kΩ | 22nF | 47p F |
| 5V | 47µF/6.3V/30mΩ | 51kΩ | 22nF | 47pF |

* $C_{COMP2}$ is needed for high ESR output capacitor.
$C_{COMP2} \leq$ 47pF is recommended.

**CC Loop Stability**

The constant-current control loop is internally compensated over the 1500mA-3000mA output range. No additional external compensation is required to stabilize the CC current.

**Output Cable Resistance Compensation**

To compensate for resistive voltage drop across the charger's output cable, the 4523K integrates a simple, user-programmable cable voltage drop compensation using the impedance at the FB pin.

Use the curve in Figure 5 to choose the proper feedback resistance values for cable compensation.

$R_{FB1}$ is the high side resistor of voltage divider. In the case of high $R_{FB1}$ used, the frequency compensation needs to be adjusted correspondingly. As show in Figure 6, adding a capacitor in parallel with $R_{FB1}$ or increasing the compensation capacitance at COMP pin helps the system stability.

**Figure 5**

**Cable Compensation at Various Resistor Divider Values**

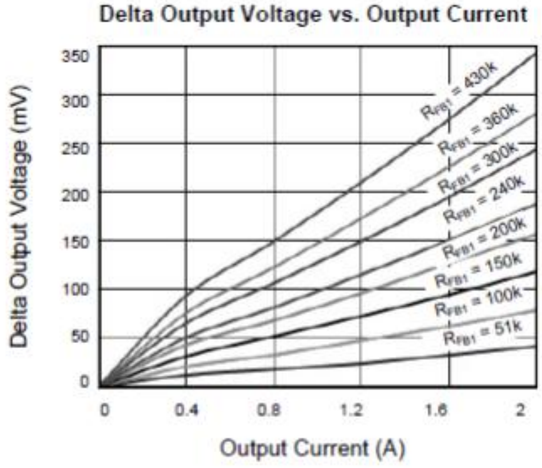
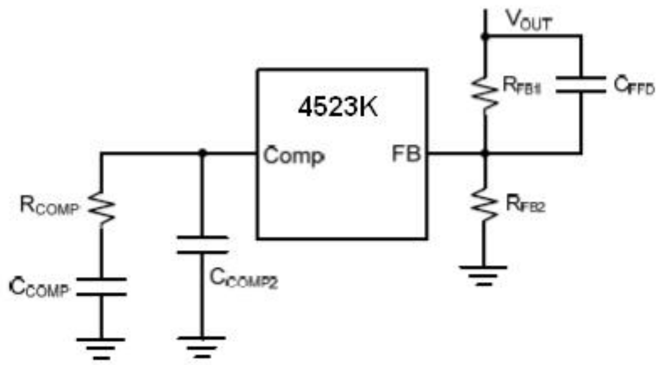


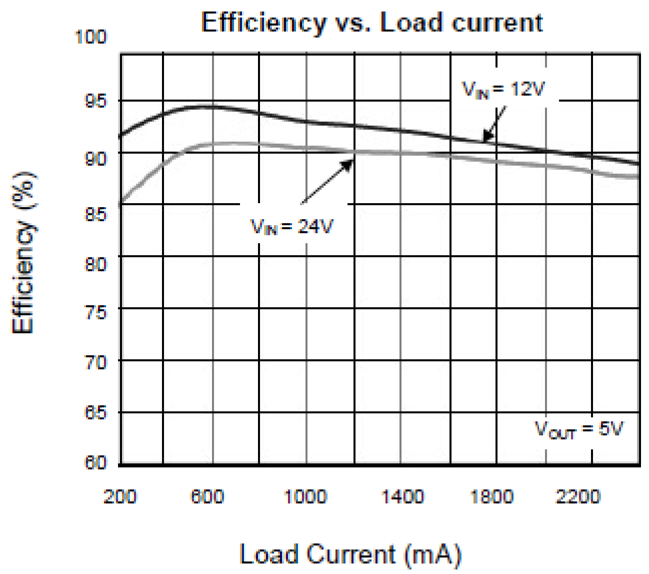

**Figure 6**

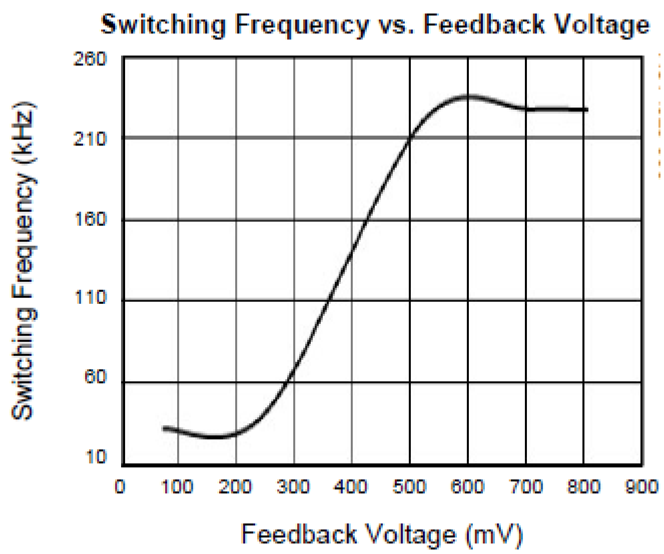
**Frequency Compensation for High $R_{FB1}$**

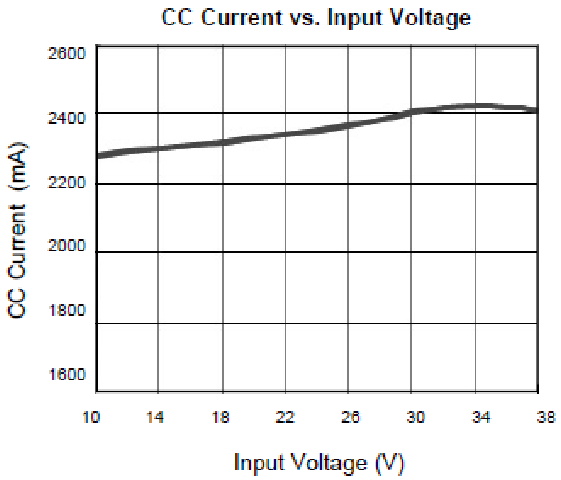


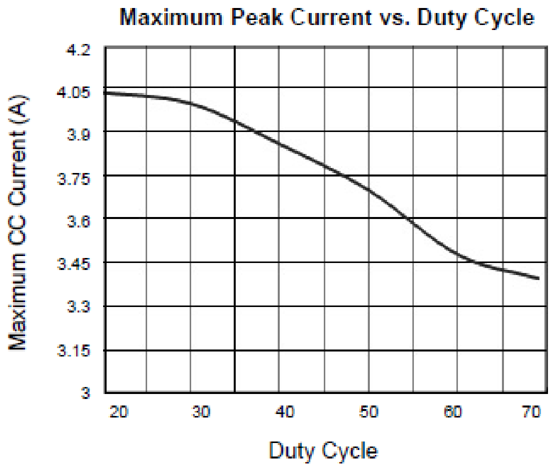
## TYPICAL PERFORMANCE CHARACTERISTICS

($L$ = 33μH, $C_{IN}$ = 10μF, $C_{OUT}$ = 47μF, $T_A$ = 25°C, $R_{COMP}$ = 8.2k, $C_{COMP1}$ = 2.2nF, $C_{COMP2}$ = NC)

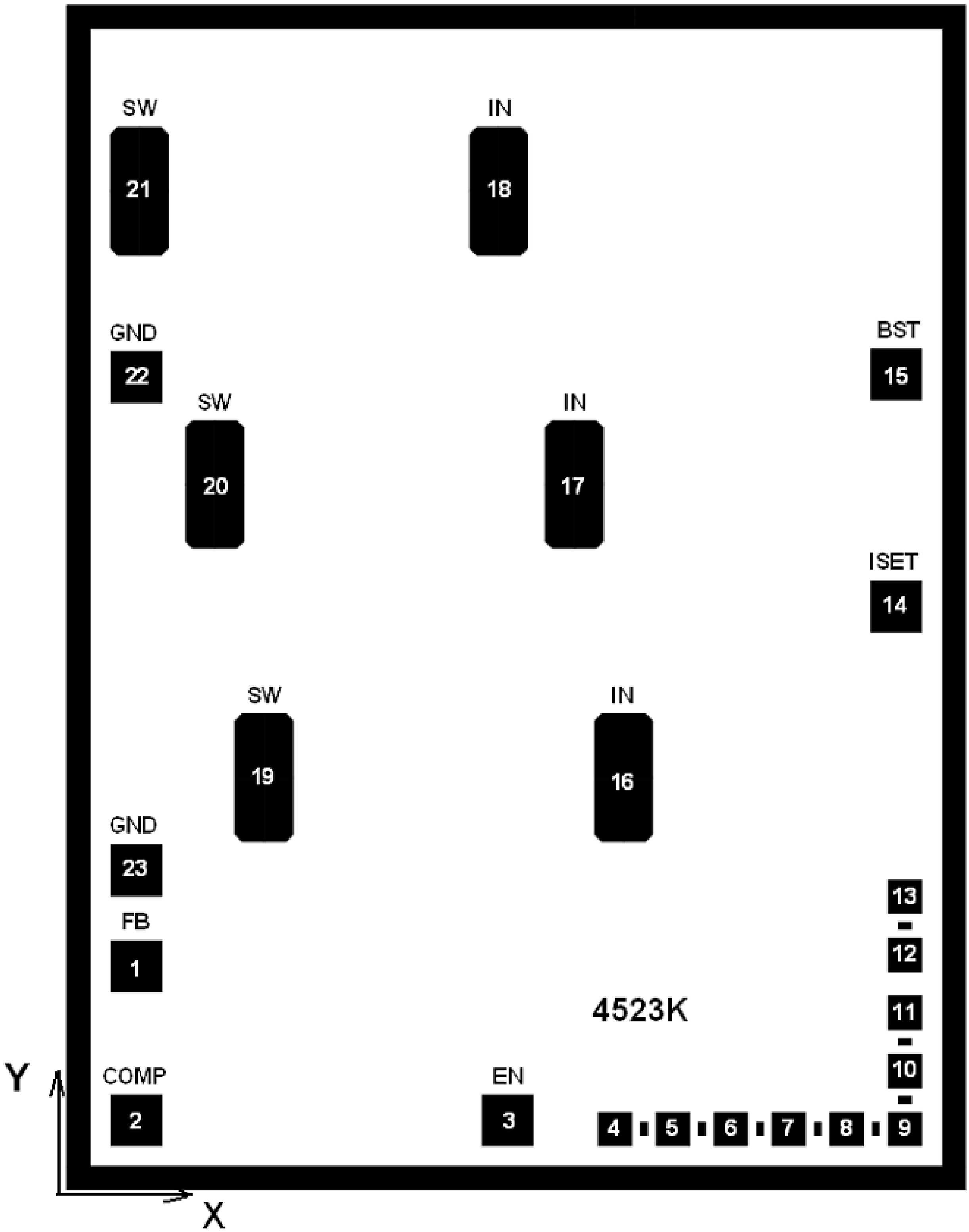



CC Current vs. Input Voltage
CC Current (mA)
2600
2400
2200
2000
1800
1600
10
14
18
22
26
30
34
38
Input Voltage (V)


Maximum Peak Current vs. Duty Cycle
Maximum CC Current (A)
4.2
4.05
3.9
3.75
3.6
3.45
3.3
3.15
3
20
30
40
50
60
70
Duty Cycle

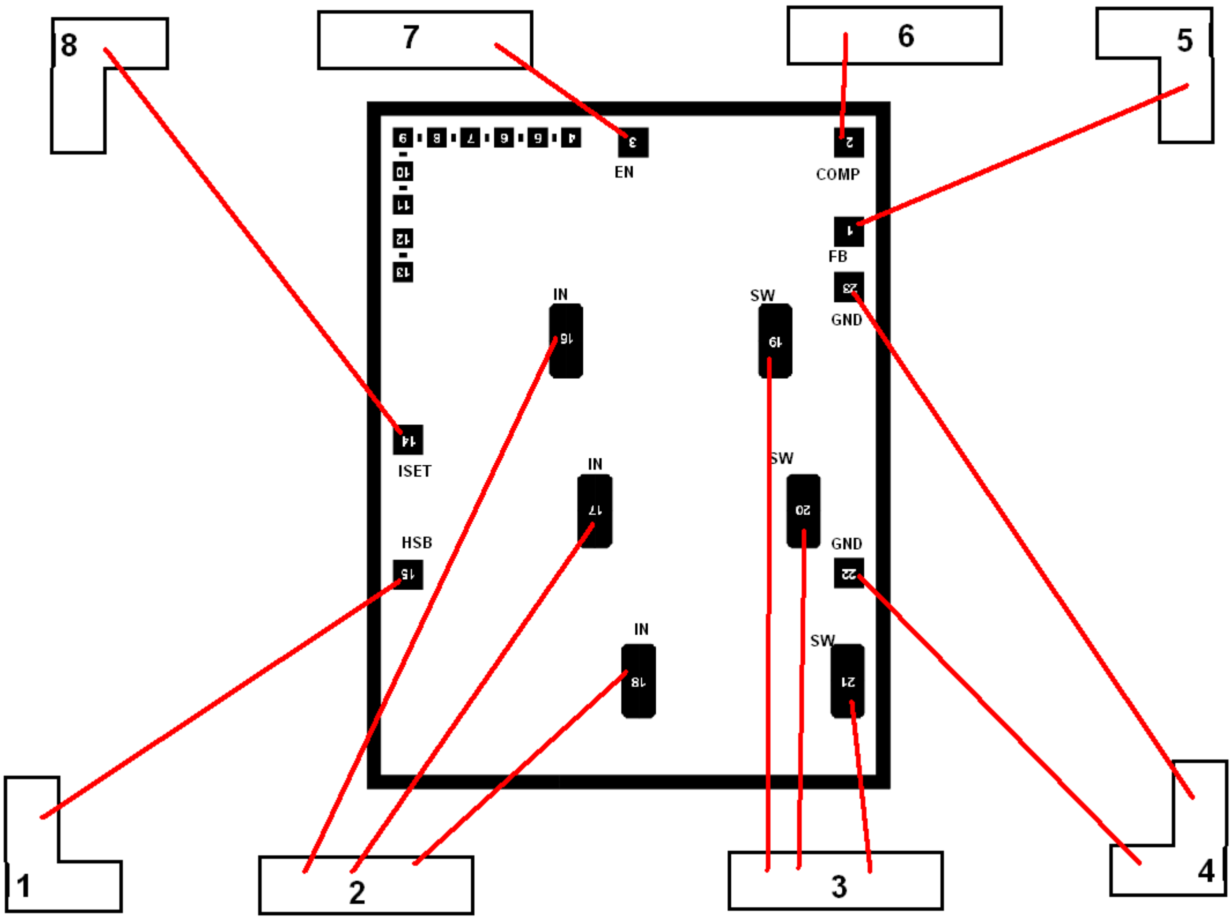
**4523K PAD LOCATION AND COORDINATES**




**Chip Size = 1.65*2.05mm$^2$**

| Chip Pad № | Pin № | Name in package | Pad Size (passivation), µm | Pad Coordinates, µm | |
|---|---|---|---|---|---|
| | | | | x | y |
| 01 | 05 | FB | 90x90 | 120 | 390 |
| 02 | 06 | COMP | 90x90 | 120 | 120 |
| 03 | 07 | EN | 90x90 | 875 | 120 |
| 04 | – | – | 60x60 | 1045 | 105 |
| 05 | – | – | 60x60 | 1145 | 105 |
| 06 | – | – | 60x60 | 1245 | 105 |
| 07 | – | – | 60x60 | 1345 | 105 |
| 08 | – | – | 60x60 | 1445 | 105 |
| 09 | – | – | 60x60 | 1545 | 105 |
| 10 | – | – | 60x60 | 1545 | 205 |
| 11 | – | – | 60x60 | 1545 | 305 |
| 12 | – | – | 60x60 | 1545 | 405 |
| 13 | – | – | 60x60 | 1545 | 505 |
| 14 | 08 | ISET | 90x90 | 1530 | 1010 |
| 15 | 01 | HSB | 90x90 | 1430 | 1490 |
| 16 | 02 | IN | 100x220 | 960 | 705 |
| 17 | 02 | | 100x220 | 870 | 1200 |
| 18 | 02 | | 100x220 | 750 | 1730 |
| 19 | 03 | SW | 100x220 | 340 | 705 |
| 20 | 03 | | 100x220 | 250 | 1200 |
| 21 | 03 | | 100x220 | 130 | 1730 |
| 22 | 04 | GND | 90x90 | 120 | 1005 |
| 23 | 04 | | 90x90 | 120 | 540 |

## BONDING DIAGRAM




Wire bonding - ∅30.5µm

PAD material – Al-Si(1%)-Ti(0.5%), thickness =2.6µm

The appearance complies with the requirements of the company standards.