34063M4K **DC-to-DC Converter Control Circuits**

September 2011 – revised July 2014

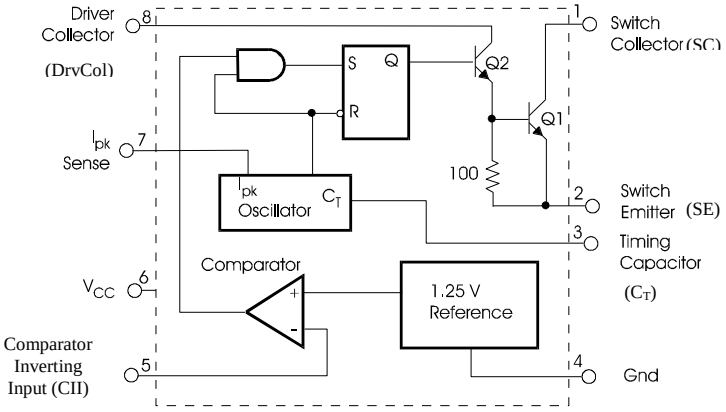
DESCRIPTION

The 34063M4K series is a monolithic control circuit containing primary functions required for DC-to-DC converters. These devices consist of an internal temperature-compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in step-down and step-up and voltage-inverting applications with a minimum number of external components.

FEATURES

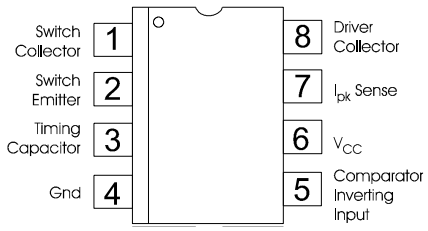
- Operation from 3.0V to 40V input
- Low standby current
- Current limiting
- Output switch current up to 1.5A
- Adjustable output voltage
- Operation at frequencies up to 100kHz
- Precision reference (2%)
- Continuous Load Current up to 1.1A (V_{in} =12 to 24V, Rcs≥0.2Ω, DIP-8 package, see Note for Step-Down Application)

SCHEMATIC DIAGRAM



(Bottom view)

PIN CONNECTIONS



(Top view)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power supply voltage	V_{CC}	40	V
Comparator input voltage range	V_{IR}	-0.3 to +40	V
Switch collector voltage	$V_{C(Switch)}$	40	V
Switch emitter voltage (V_{Pin1}=40V)	$V_{E(Switch)}$	40	V
Switch collector-to-emitter voltage	$V_{CE(Switch)}$	40	V
Driver collector voltage	$V_{C(Driver)}$	40	V
Driver collector current (Note 1)	$I_{C(Driver)}$	100	mA
Switch current	I_{Sw}	1.5	A
Operating junction temperature	T_J	+150	°C
Operating ambient temperature range	T_A	-40 to +85	°C
Storage temperature range	T_{STG}	-65 to + 150	°C
ESD (HBM)		2500	V

ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V, T_A=T_{Low} to T_{High}, unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (V_{Pin5}=0V, C_T=1.0nF, T_A=25°C)	f_{osc}	24	33	42	kHz
Charge current (V_{CC}=5.0V to 40V, T_A=25°C)	I_{chg}	24	35	42	µA
Discharge current (V_{CC}=5.0V to 40V, T_A=25°C)	I_{dischg}	140	220	260	µA
Discharge-to-charge current ratio (Pin7 to V_{CC}, T_A=25°C)	I_{dischg}/I_{chg}	5.2	6.5	7.5	-
Current limit sense voltage (I_{chg}=I_{dischg}, T_A=25°C)	$V_{Ipk(sense)}$	250	300	350	mV
OUTPUT SWITCH (Note 2)					
Saturation voltage, Darlington connection I_{Sw}=1.0A, Pins1, 8 connected	$V_{CE(sat)}$	-	1.0	1.3	V
Saturation voltage, Darlington connection (I_{Sw}=1.0A, R_{Pin8}=82Ω to V_{CC}, forced β=20)	$V_{CE(sat)}$	-	0.45	0.7	V
DC current gain (I_{Sw}=1.0A, V_{CE}=5.0, T_A=25°C)	h_{FE}	50	75	-	-
Collector off-state current (V_{CE}=40V)	$I_{C(off)}$	-	1.0	100	µA
COMPARATOR					
Threshold voltage	V_{th}	1.225 1.21	1.25 -	1.275 1.29	V
Threshold voltage line regulation (V_{CC}=3.0V to 40V)	Reg_{line}	-	1.4	5.0	mV
Input bias current (V_{in}=0V)	I_{IB}	-	-20	-400	nA
TOTAL DEVICE					
Supply current (V_{CC}=5.0V to 40V, C_T=1.0nF, Pin7=V_{CC}, V_{Pin5}>V_{th}, Pin2 =Gnd, remaining pins - open	I_{CC}	-	-	4.0	mA

Notes:

1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during the test to maintain the junction temperature as close to the ambient temperature as possible.

TYPICAL PERFORMANCE CHARACTERISTICS

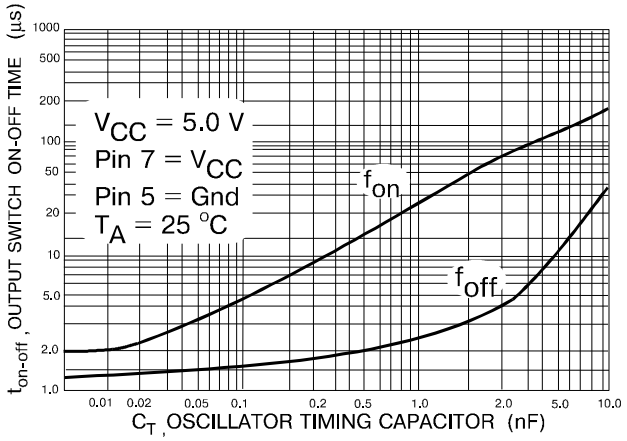


Fig.1. Output Switch on-off time versus Oscillator timing capacitor

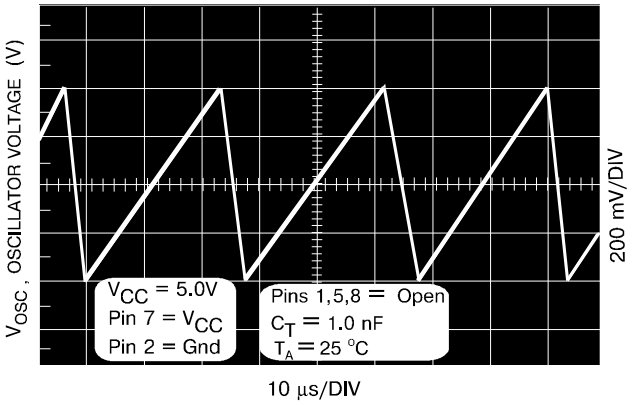


Fig.2. Timing capacitor waveform

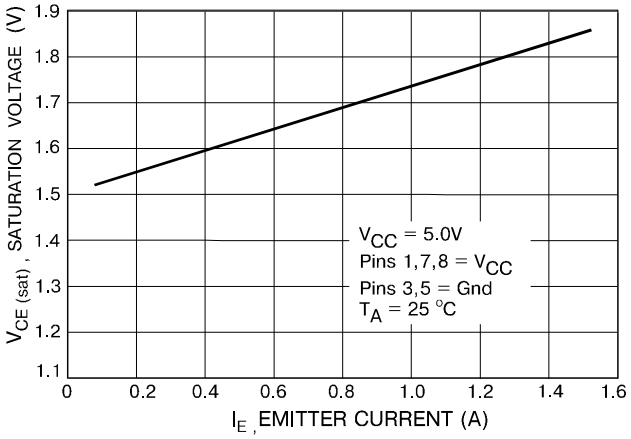


Fig.3. Emitter follower configuration output saturation voltage versus Emitter current

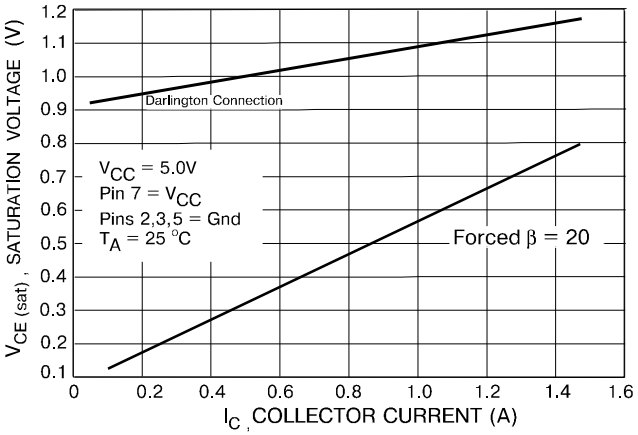


Fig.4. Common emitter configuration output saturation voltage versus Collector current

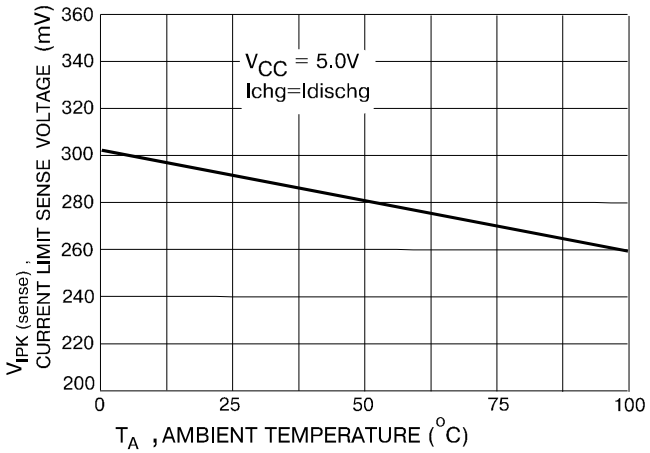


Fig.5. Current limit sense voltage versus Temperature

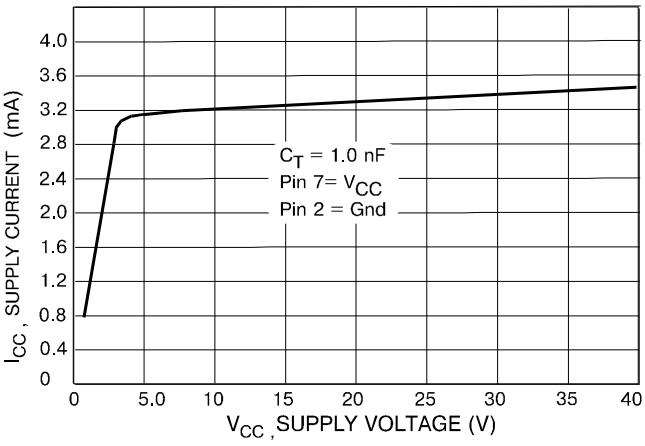


Fig.6. Standby supply current versus Supply voltage

APPLICATION INFORMATION

Fig.1. Step–up converter

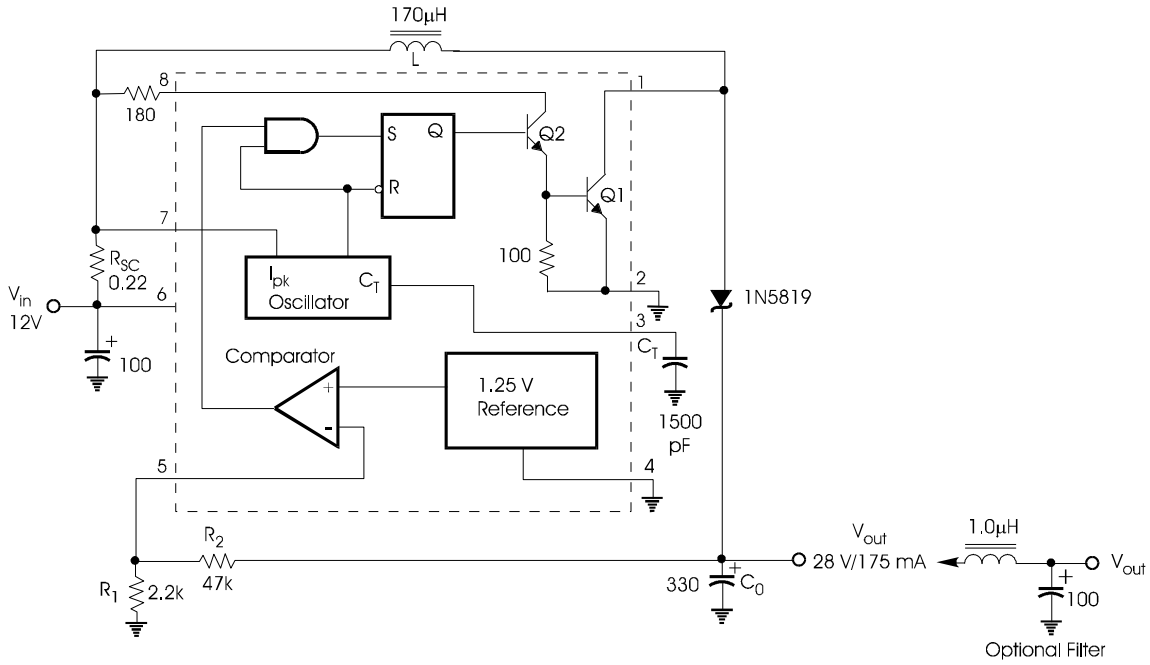
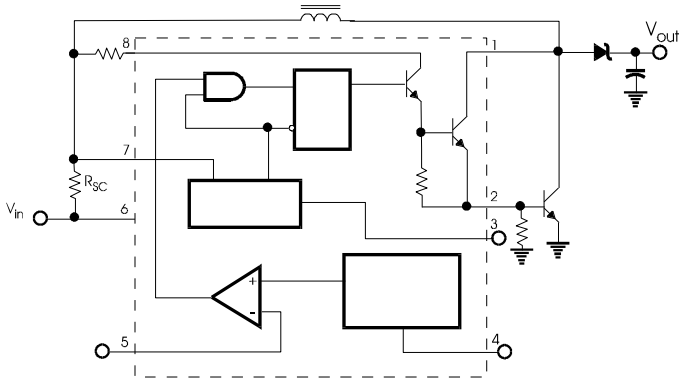
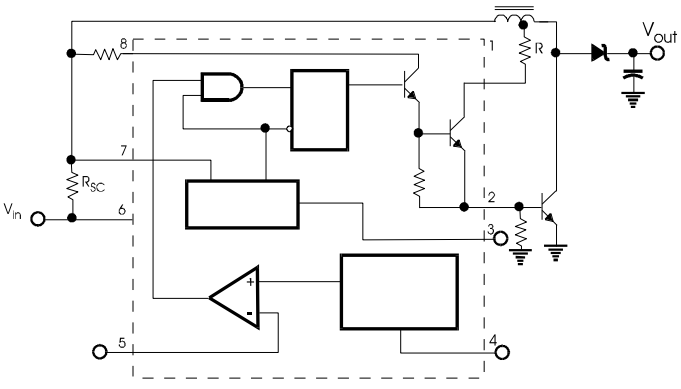


Fig.2. External current boost connections for $I_{C\ Peak}$ greater than 1.5A

2a. External NPN switch

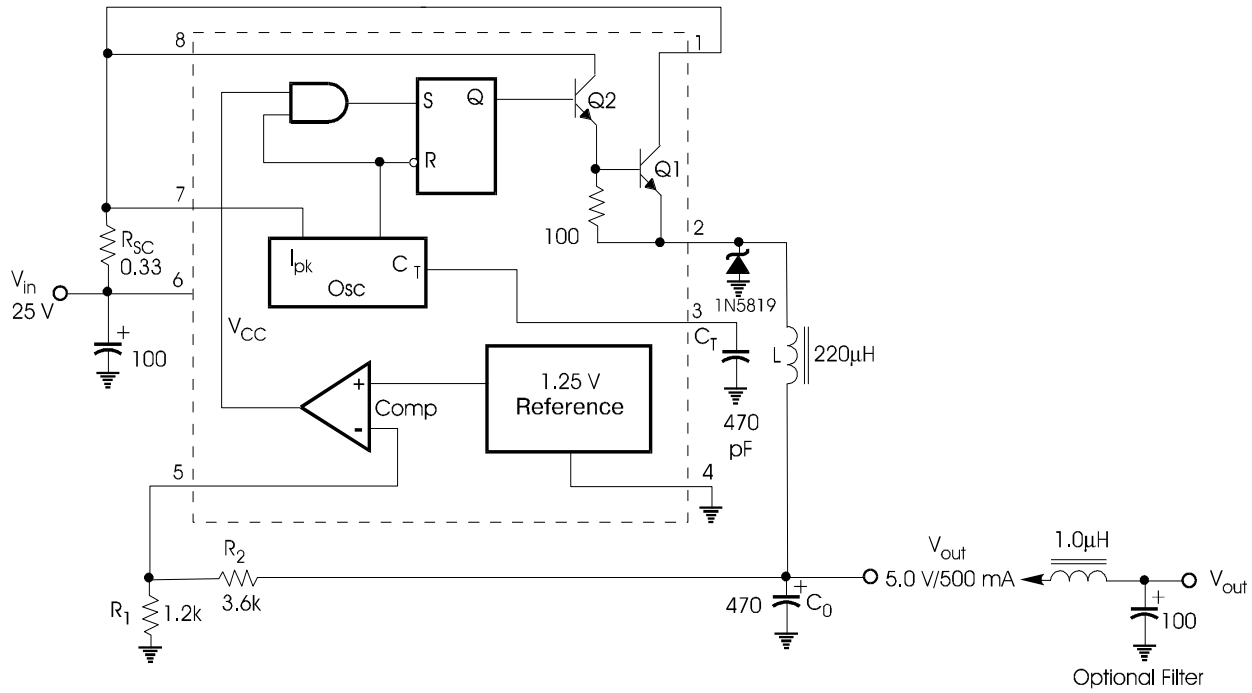


2b. External NPN saturated switch



Note: R to 0 at constant V_{IN}

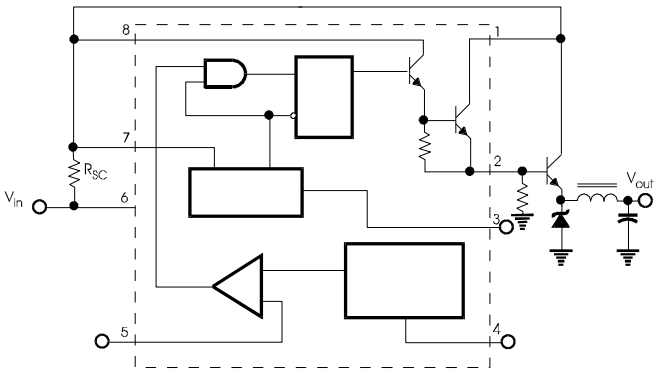
Fig.3. Step-down Converter



Note: It is recommended to use L=165uH, Ct=1nF, Rcs=0.2 Ohm for Load Current 1.1A. If Rcs≤0.2Ω then the IC could be damaged (the short circuit of collector-emitter)

Fig.4. External current boost connections for $I_{C\ Peak}$ greater than 1.5A

4a. External NPN switch



4b. External PNP saturated switch

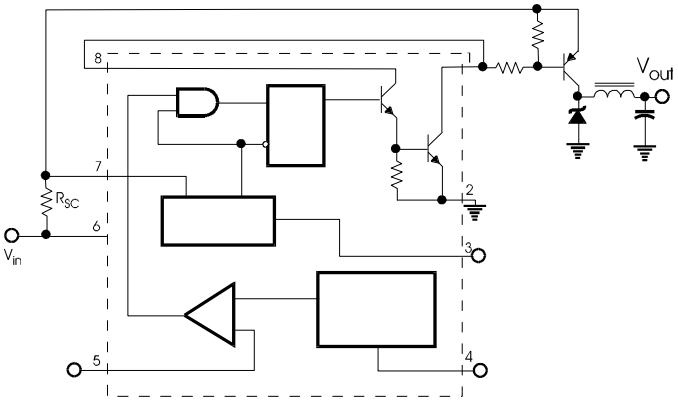


Fig.5. Voltage inverting converter

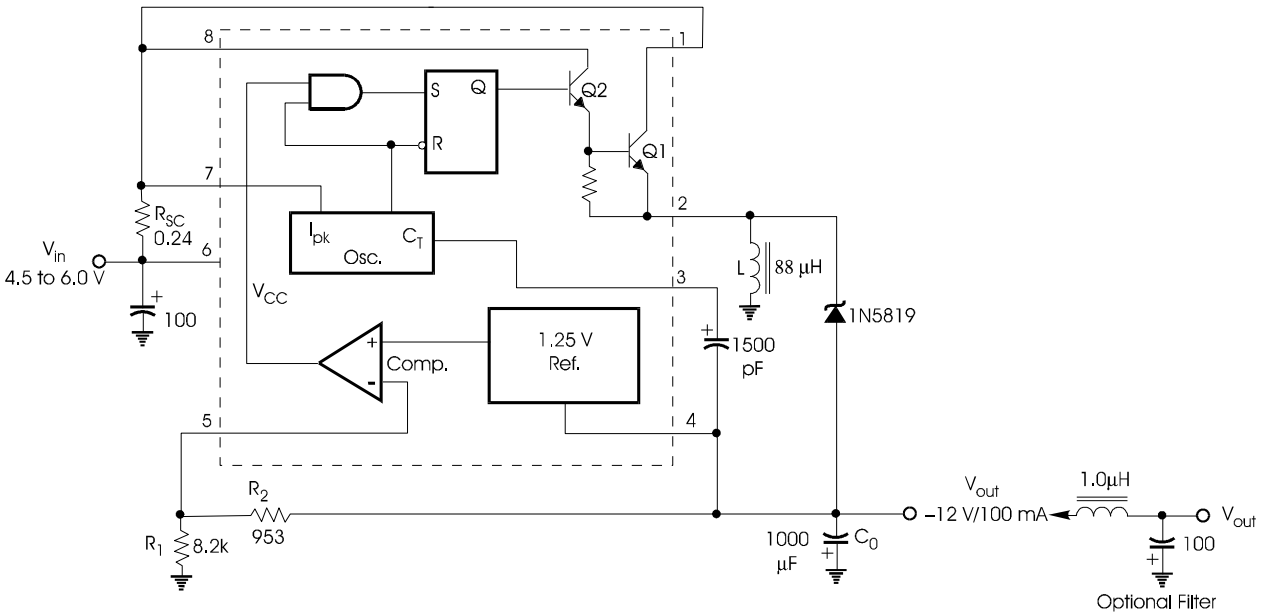
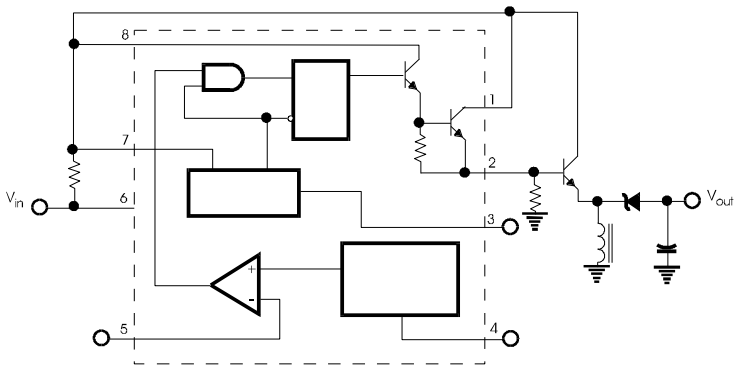
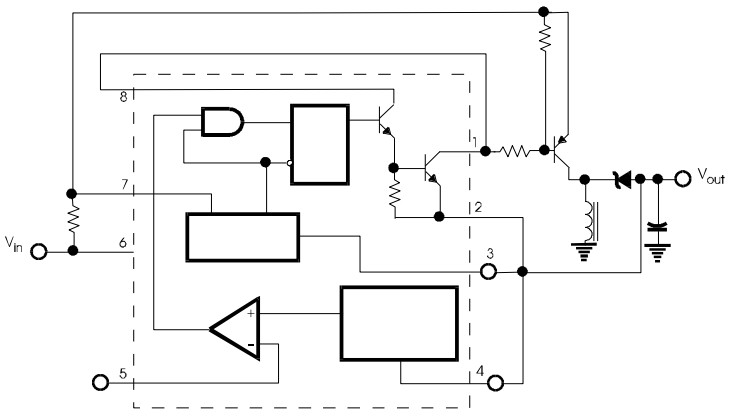


Fig.6. External current boost connections for $I_{C\ Peak}$ greater than 1.5A

6a. External NPN switch



6b. External PNP saturated switch



TABLE

DESIGN FORMULA

Calculation	Step-up	Step-down	Voltage-inverting
t_{on}	$\frac{V_{out}+V_F-V_{in(\min)}}{V_{in(\min)}-V_{sat}}$	$\frac{V_{out}+V_F}{V_{in(\min)}-V_{sat}-V_{out}}$	$\frac{\lvert V_{out}\rvert+V_F}{V_{in}+V_{sat}}$
$(t_{on}+t_{off})$max	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4.0 \times 10^{-5}\, t_{on}$	$4.0 \times 10^{-5}\, t_{on}$	$4.0 \times 10^{-5}\, t_{on}$
$I_{pk(switch)}$	$2I_{out(\max)}\left(\frac{t_{on}}{t_{off}}+1\right)$	$2I_{out(\max)}$	$2I_{out(\max)}\left(\frac{t_{on}}{t_{off}}+1\right)$
R_{sc}	$0.3/I_{pk(Switch)}$	$0.3/I_{pk(Switch)}$	$0.3/I_{pk(Switch)}$
$L_{(min)}$	$\left(\frac{V_{in(\min)}-V_{sat}}{I_{pk(switch)}}\right)\times t_{on(\max)}$	$\left(\frac{V_{in(\min)}-V_{sat}-V_{out}}{I_{pk(switch)}}\right)\times t_{on(\max)}$	$\left(\frac{V_{in(\min)}-V_{sat}}{I_{pk(switch)}}\right)\times t_{on(\max)}$
C_o	$9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{on}+t_{off})}{8V_{ripple(pp)}}$	$9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$

TERMS AND DEFINITIONS

V_{sat} – Saturation voltage of the output switch.

V_F– Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

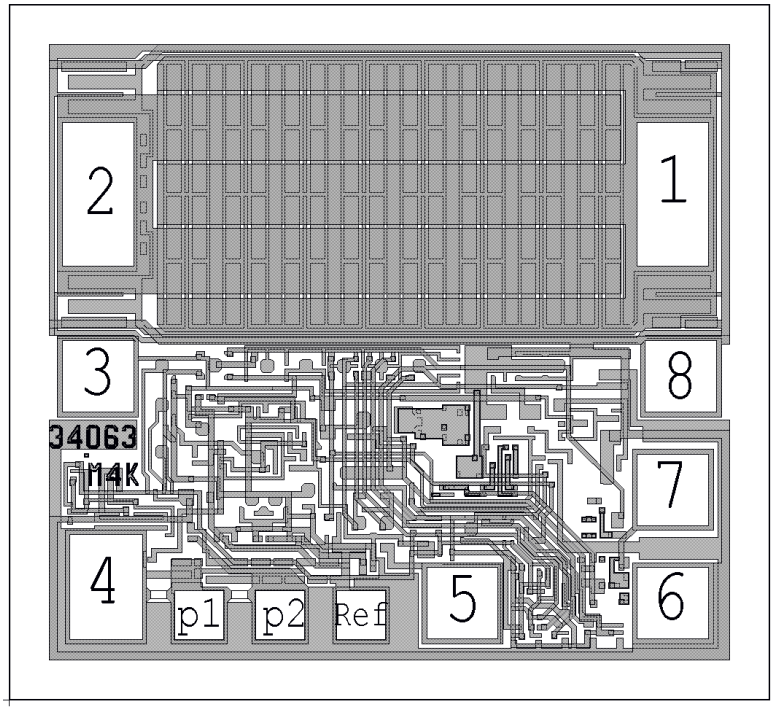
V_{in} – Nominal input voltage.

V_{out} – Desired output voltage, $|V_{out}|=1.25\left(1+\frac{R_2}{R_1}\right)$

f_{min} – Minimum desired output switching frequency at the selected values of V_{in} and I_{out}.

$V_{ripple(p-p)}$ – Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

34063M4K
Pad location



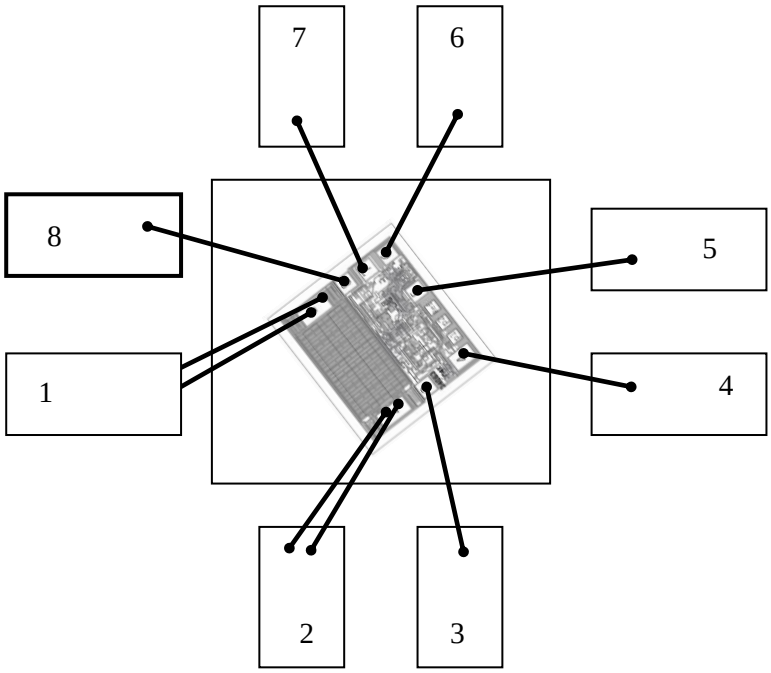
Chip size: 0.94 x 0.86 mm²

PAD	PIN	NAME	Pad center coordinates, μm		Pad (opening) size, μm	
			X	Y	W	H
1	1	Switch Collector	820	625	88	178
2	2	Switch Emitter	110	625	88	178
3	3	Timing Capacitor	110	400	88	88
4	4	GND	120	140	90	130
5	5	Comparator Inverting Input	560	120	88	88
6	6	Vcc	820	120	88	88
7	7	Ipk Sense	820	260	88	88
8	8	Driver Collector	830	400	88	88

Note: 1. Pad 1 and Pad 2 should be connected with two bonding wires (each).
2. Pads metal thickness is 2.25μm±10%.

BONDING DIAGRAM

DIP8, SO8 Packages



The appearance complies with the requirements of the company standards.