Inv № 533

34063CM3K 1.2A STEP-DOWN / STEP-UP / INVERTING DC-DC CONVERTER

July 2009 – revised July 2014

DESCRIPTION

The 34063CM3K is a monolithic switching regulator control circuit containing the primary functions required for DC-DC converters. This device consists of internal temperature compensated reference, voltage comparator, controlled duty cycle oscillator with active current limit circuit, driver and high current output switch. The device is specifically designed to be used in Step-Down, Step-Up and Voltage-Inverting applications with a minimum number of external components.

The 34063CM3K is the enhanced version of MC34063A with the ability to work in higher frequency.

The 34063CM3K is available in 2 packages: SOP- 8 and DIP-8.

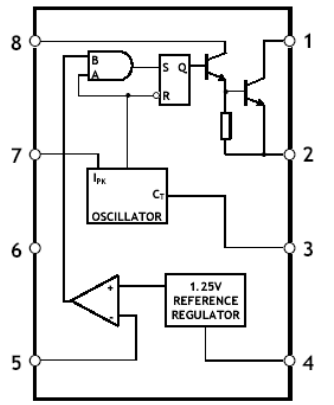
FEATURES

- Operation from 3V to 40V
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.2A
- Output Voltage Adjustable
- Operation Frequency up to 180 kHz (C_T = 100pF)
- Precision 2% Reference
- Continuous Load Current up to 0.75A(V_{in} =12 to 24V, Rcs≥0.2Ω, DIP-8 package, see Note for Step-Down Application)

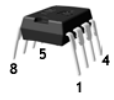
APPLICATIONS

- Battery Chargers
- NICs/Switches/Hubs
- ADSL Modems
- Negative Voltage Power Supplies

SCHEMATIC DIAGRAM AND PIN DESCRIPTION



PIN 1	Switch Collector	Internal switch transistor collector	DIP-8
PIN 2	Switch Emitter	Internal switch transistor emitter	
PIN 3	Timing Capacitor	Timing Capacitor to control the switching frequency	
PIN 4	GND	Ground pin for all internal circuits	
PIN 5	Comparator Inverting Input	Inverting input pin for internal comparator	
PIN 6	V_{CC}	Voltage supply	SOP-8
PIN 7	I_{PK} Sense	Peak Current Sense Input by monitoring the voltage drop across an external I sense resistor to limit the peak current through the switch	
PIN 8	Driver Collector	Voltage driver collector	



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	Supply Voltage	3	40	V
T_A	Ambient Temperature	-40	85	°C

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

SYMBOL	PARAMETER		VALUE	UNIT
V_{CC}	Power Supply Voltage		40	V
V_{IR}	Comparator Input Voltage Range		-0.3 to 40	V
V_C (SWITCH)	Switch Collector Voltage		40	V
V_E (SWITCH)	Switch Emitter Voltage (Vpin1= 40V)		40	V
V_{CE} (SWITCH)	Switch Collector to Emitter Voltage		40	V
V_C (DRIVER)	Driver Collector Voltage		40	V
I_C (DRIVER)	Driver Collector Current (NOTE 2)		100	mA
I_{SW}	Switch Current		1.2	A
POWER DISSIPATION AND THERMAL CHARACTERISTICS				
P_D	DIP Package	Power Dissipation (T_A= 25°C)	1.25	W
$R_{\Theta JA}$		Thermal Resistance	100	°C/W
P_D	SOP Package	Power Dissipation (T_A= 25°C)	625	mW
$R_{\Theta JA}$		Thermal Resistance	160	°C/W
T_J	Operating Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-65 to 150	°C
ESD for 34063CM3K			3000	V

SEE NOTES ON THE NEXT PAGE ...

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, **T_A** = -40 TO 85°C, UNLESS OTHERWISE SPECIFIED

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OSCILLATOR						
F_{OSC}	Frequency	Vpin5 = 0V; T_A = 25°C; C_T = 1 nF	30	38	45	kHz
I_{CHG}	Charge Current	V_{CC} = 5.0V to 40V; T_A = 25°C	30	38	45	µA
I_{DISCHG}	Discharge Current	V_{CC} = 5.0V to 40V; T_A = 25°C	180	240	290	µA
I_{DISCHG}/I_{CHG}	Discharge to Charge Current Ratio	Pin 7 to V_{CC} ; T_A = 25°C	5.2	6.5	7.5	-
$V_{IPK(SENCE)}$	Current Limit Sense Voltage	I_{CHG} = I_{DISCHG}; T_A = 25°C	250	300	350	mV
OUTPUT SWITCH (NOTE 3)						
$V_{CE(SAT)}$	Saturation Voltage, Darlington connection	I_{SW} = 0.8A; Pins 1,8 connected	-	1.0	1.3	V
$V_{CE(SAT)}$	Saturation Voltage (see NOTE 4)	I_{SW} = 0.8 A; Rpin 8 = 82Ω to V_{CC}; Forced β = 20	-	0.45	0.8	V
h_{FE}	DC Current Gain	I_{SW} = 0.8 A; V_{CE} = 5.0 V T_A = 25°C	50	75	-	-
$I_{C(OFF)}$	Collector Off-State Current	V_{CE} = 40 V	-	0.01	100	µA
COMPARATOR						
V_{TH}	Threshold Voltage	T_A = 25°C	1.225	1.25	1.275	V
		T_A= -40°C to +85°C	1.210		1.290	
REG_{LINE}	Threshold Voltage Line Regulation	V_{CC} = 3V to 40 V	-	1.4	5	mV
I_{IB}	Input Bias Current	V_{IN} = 0 V	-	-20	-400	nA
TOTAL DEVICE						
I_{CC}	Supply Current	V_{CC} = 5.0 V to 40 V; C_T = 1.0 nF; Pin 7 = V_{CC}; Vpin 5 > Vth; Pin 2 = GND; other pins open	-	-	4	mA

SEE NOTES ON THE NEXT PAGE ...

ELECTRICAL CHARACTERISTICS (CONTINUED)

NOTES

1: Stresses greater than those listed under «Absolute Maximum Ratings» may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under «Recommended Operating Conditions» is not implied. Exposure to «Absolute Maximum Ratings» for extended periods may affect device reliability.

2: Maximum package power dissipation limits must be observed.

3: Low duty cycle pulse technique are used during test to maintain junction temperature as close to ambient temperature as possible.

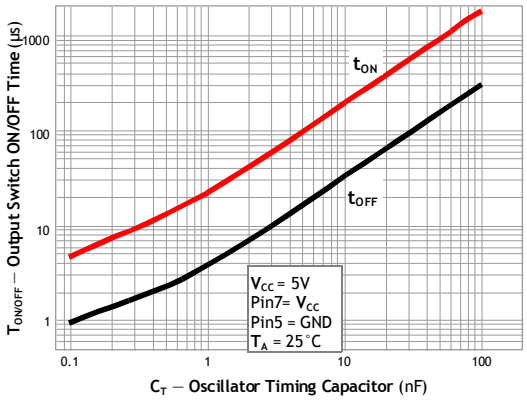
4: If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents (≤ 300mA) and high driver currents (≥ 30mA), it may take up to 2.0µs for it to come out of saturation. This condition will shorten the off time at frequencies 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended:

Forced β of output switch: $$\frac{I_{C(OUTPUT)}}{I_{C(DRIVER)} - 7.0mA*} \geq 10$$

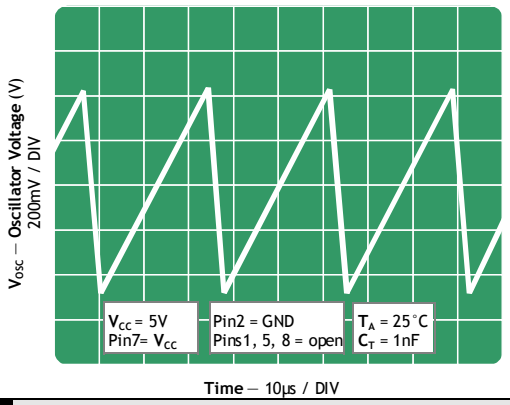
***** The 100Ω resistor in the emitter of the driver device requires about 7 mA before the output switch conducts.

TYPICAL PERFORMANCE CHARACTERISTICS

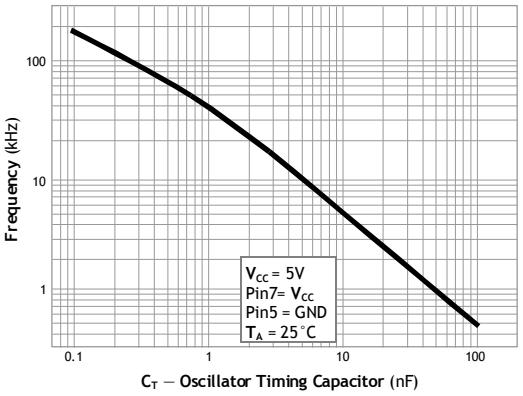
A — OUTPUT SWITCH ON-OFF TIME versus OSCILLATOR TIMING CAPACITOR



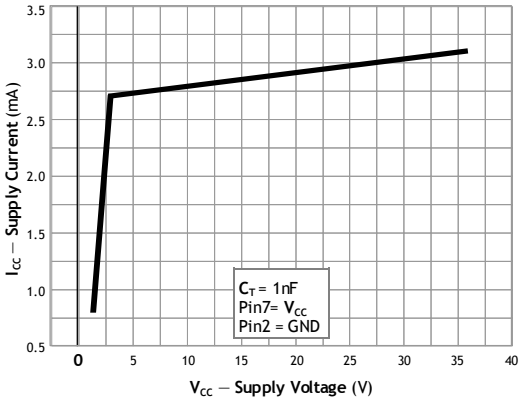
B — TIMING CAPACITOR WAVEFORM



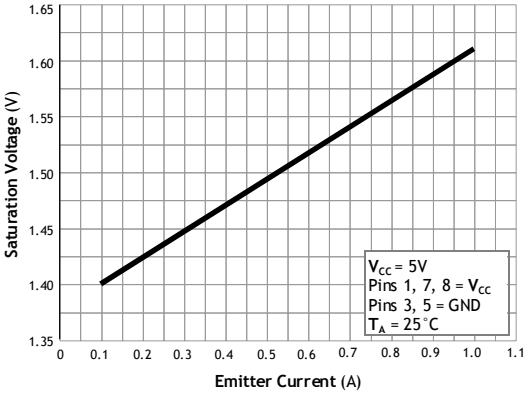
C — OSCILLATOR FREQUENCY versus TIMING CAPACITOR



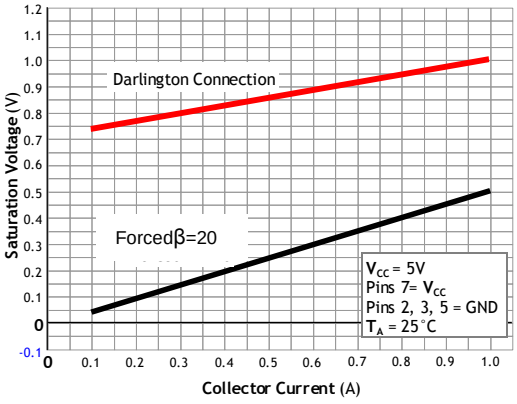
D — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE



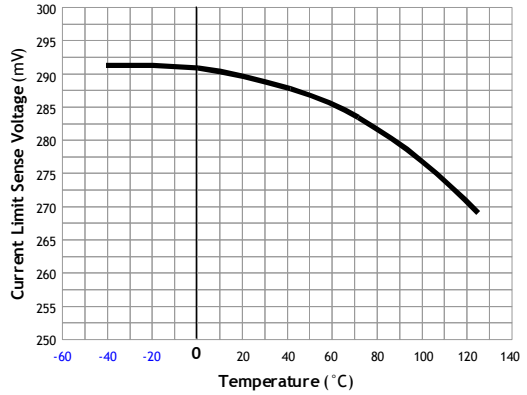
E — EMITTER FOLLOWER CONFIGURATION OUTPUT SATURATION VOLTAGE vs. EMITTER CURRENT



F — COMMON EMITTER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE vs. COLLECTOR CURRENT

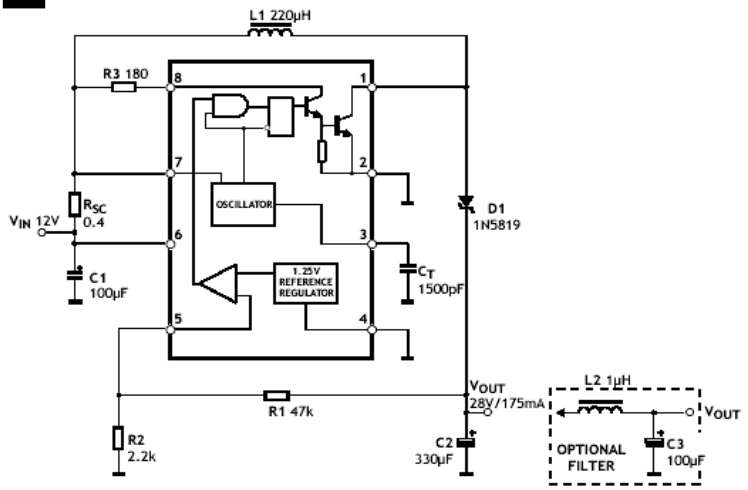


G — CURRENT LIMIT SENSE VOLTAGE versus TEMPERATURE



TYPICAL APPLICATIONS

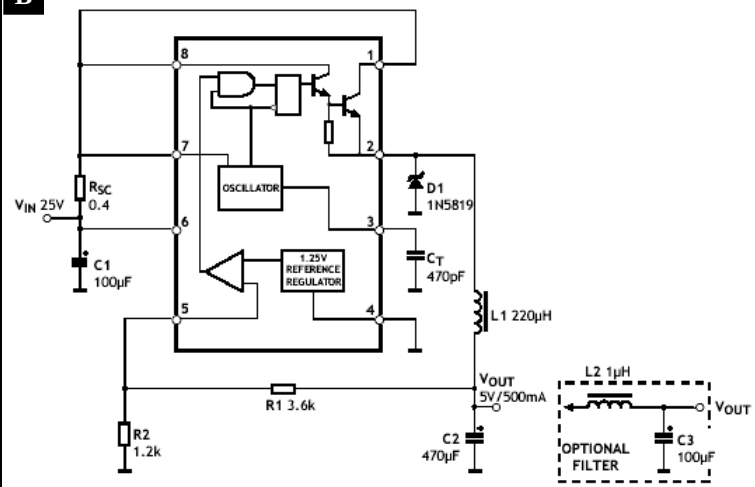
A STEP-UP CONVERTER



This is a typical step-up converter configuration. In the steady state, if the resistor divider voltage at pin 5 is greater than the voltage in the non-inverting input, which is 1.25V deter-mined by the internal reference, the output of the comparator will go low. At the next switching period, the output switch will not conduct and the output voltage will eventually drop below its nominal voltage until the divider voltage at pin 5 is lower than 1.25V.

Then the output of the comparator will go high, the output switch will be allowed to conduct. Since
Vpin5 = V_{OUT} * R2/(R1+R2) = 1.25(V), the output voltage can be decided by
V_{OUT} = 1.25 * (R1+R2)/R2 (V).

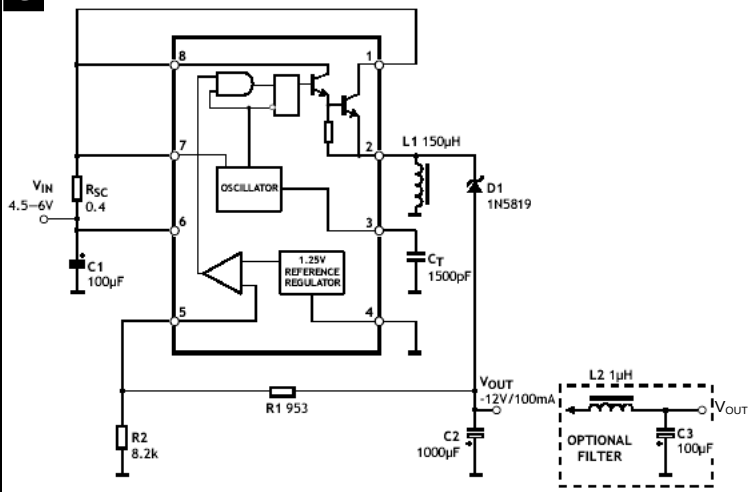
B STEP-DOWN CONVERTER



This is a typical step-down converter configuration. The working process in the steady state is similar to step-up converter,
Vpin5 = V_{OUT} * R2/(R1+R2) = 1.25 (V),
the output voltage can be decided by
V_{OUT} = 1.25 * (R1+R2)/R2 (V).

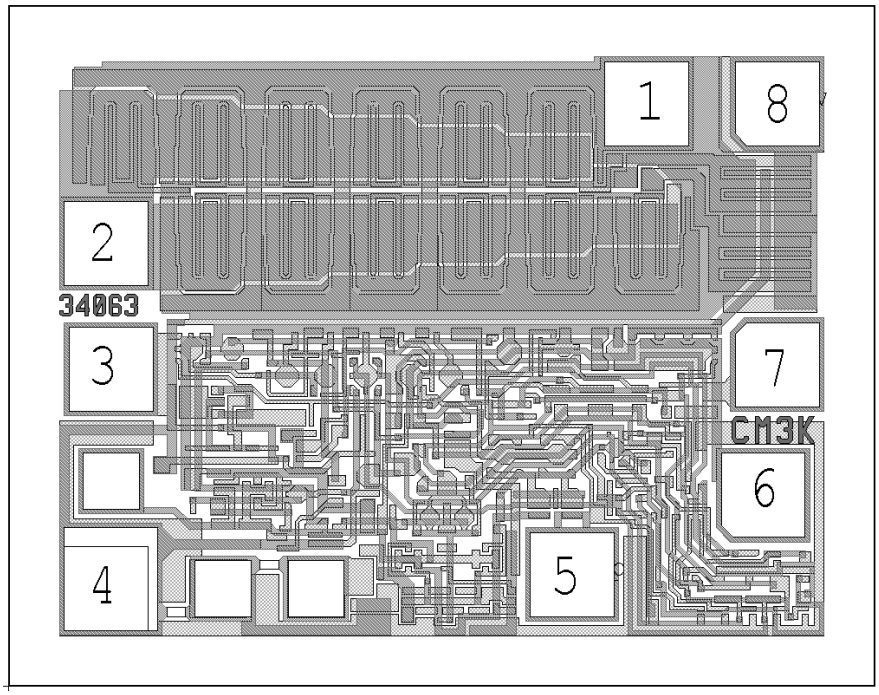
Note: It is recommended to use L=165uH, Ct=1nF, Rcs=0.2 Ohm for Load Current 0.75A.
If Rcs≤0.2Ω then the IC could be damaged (the short circuit of collector-emitter)

C VOLTAGE INVERTING CONVERTER



This is a typical inverting converter configuration. The working process in the steady state is similar to step-up converter, the difference in this situation is that the voltage at the non-inverting pin of the comparator is equal to 1.25V+V_{OUT}, then
Vpin5=V_{OUT} * R2/(R1+R2) = 1.25V+V_{OUT},
so the output voltage can be decided by
V_{OUT} = -1.25 * (R1+R2)/R1 (V).

PAD LOCATION 34063CM3K



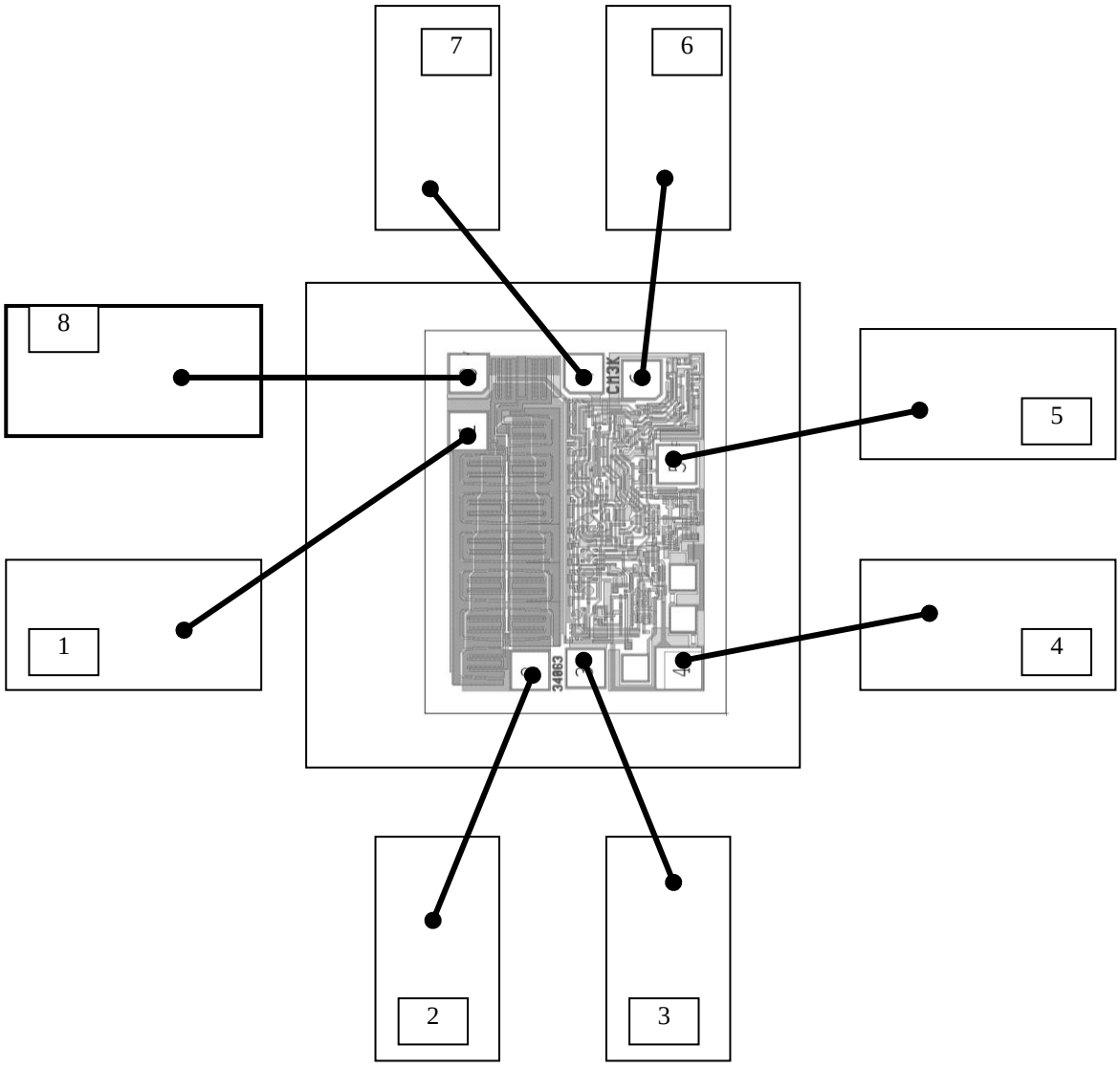
Chip size: 0.93 x 0.73 mm^2

Pad Location Coordinates

Pad #	Pin #	Pin Name	Description	Center Coordinates		Pad Size	
				X	Y	W	H
1	1	SC	Switch Collector	685	625	90	90
2	2	SE	Switch Emitter	105	475	90	90
3	3	Tc	Timing Capacitor	110	340	90	90
4	4	GND	GND	110	115	100	110
5	5	CII	Comparator Inverting Input	605	120	90	90
6	6	Vcc	Vcc	810	205	90	90
7	7	$I_{PK}S$	Ipk Sense	825	345	90	90
8	8	DRVCOL	Driver Collector	825	625	90	90

Note : Metal thickness at the PAD is 2.25um ±10%

Bonding Diagram
Package DIP-8, SO-8



The appearance complies with the requirements of the company standards.